Plessey PR2250

communication receiver

PART 1

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PR2250G H.F. COMMUNICATIONS RECEIVER

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PLESSEY PR 2250G H.F. RECEIVER

1. INTRODUCTION

1.1 The PR 2250G is a double-superhet communications receiver providing continuous coverage of the frequency range 10 kHz to 30 MHz and designed for the reception of AM, CW, SSB, ISB, FSK and Piccolo signals.

1.2 A conventional tuning control provides continuous, fast or slow frequency control, without any need for Band-changing. In addition, a 'keypad' gives instant frequency change as required. The recall of up to sixteen frequencies, together with their respective mode, bandwidth and a.g.c settings, is also provided.

1.3 The receiver is made up of nine plug-in modules mounted within the case. The front panel and its associated control circuit panel also form a removable module. All modules form functional entities, and all can be replaced without the need for special tools, or workshop facilities.

2. BASIC TECHNICAL DESCRIPTION

2.1 The received signal from the antenna is filtered in Module 1A by a fixed 30 MHz low pass filter.

2.2 After filtering, the signal is applied to the first mixer - Module 2, via a wideband, a.g.c - controlled amplifier. The first local oscillator input to this mixer is provided by the synthesiser - Module 9 which produces a variable-frequency output of stability equal to that of the frequency standard. Frequency control is exercised by Module 10, either from the front-panel tuning controls, or from a remote position.

2.3 The 65 MHz 1st IF output from Module 2 is amplified before being applied to the second mixer - Module 3D. The 2nd local oscillator frequency is fixed at 63.6 MHz, and is also supplied by the synthesiser - Module 9. The 1.4 MHz 2nd IF bandwidth is determined by one of five crystal filters which under front-panel (or remote) control, determine reception bandwidth. These are selected by the front-panel controls - Module 10, or remotely.

2.4 The filtered 2nd IF signal is amplified with a.g.c - Module 4, and followed by the detector circuits. The signal detectors are in Module 5, and the a.g.c detector is in Module 4. The delay time constant of the a.g.c. is operator-variable.

2.5 Three signal detectors are available, an envelope detector (used in AM mode) and two product detectors (used in F, CW, P and SSB modes). The appropriate detector is selected by the operator. The product detectors also have an input from the BFO in Module 6; this input can either be:

a. Locked to the external frequency standard.

b. Varied over $\pm$ 8 kHz by the front-panel 'BFO' control.

c. Locked to an incoming pilot carrier.

For 'F' mode (fixed offset) the BFO fixed offset value is preset by switches in Module 6. The offset can be changed to suit individual operational requirements.

2.6 The detected output signal is amplified in Module 5 to give the following outputs:

a. Two independent audio "line" outputs.

b. A front-panel headphone output.

c. Two independent 100 kHz 'IF' outputs.

d. A drive for the built-in loudspeaker.

2.7 Function control of the receiver is completely digital, and is exercised by Module 10. The audio gain, BFO and RF-IF gain are all analogue controls. Manual tuning of the receiver is carried out using the front-panel controls, first by setting the frequency on the keypad, and then by tuning 'around' using a normal 'feel' manual tuning control. This is coupled to an optical encoder. Frequency readout is by an LED display, indicating to 10 Hz.

2.8 A maximum of sixteen settings of frequency, bandwidth, mode, and a.g.c. delay time-constant can be stored in the memory circuits of Module 12A, these can be used at any time.

2.9 The PR 2250G contains seven modules that plug in from the front of the unit, and two that plug in from the rear. The front panel - Module 10 - is hinged to the front of the frame.

2.10 The front-panel is in two parts, and is hinged to the frame. The associated printer-circuit panel is also hinged to the back of the front panel, so that when the front-panel is open, the printed-circuit panel can be swung downward to permit access to the rear of the front panel, and to the track side of the printed-circuit panel.

2.11 Connection between Module 10 and the remainder of the receiver is made by three flat flexible cables. One plugs into Module 12, the others plug into connectors on the main receiver frame.

2.12 The PR 2250G provides an output of the "set frequency", in a serial format compatible with the PV 2277 Mode Select Unit. This output is used to drive the preselector.

2.13 Two PR 2250G receivers can be coupled together via the Mode Select Unit PV 2277, and used in a Master - Slave configuration. Either receiver may be designated as Master.

3. FUNCTIONAL DESCRIPTION

3.1 Signal-Frequency Circuits

3.1.1 The 50 ohm antenna input is applied to filter circuits in Module 1A. The signal is fed via a low-pass filter to the RF amplifier, Module 2. This amplifier is a.g.c controlled.

3.2 1st Mixer and Local Oscillator

3.2.1 The amplified RF signal passes to the 1st mixer - Module 2. The 2nd input to the mixer is supplied from the synthesiser - Module 9A.

3.2.2 The synthesiser consists of a complex phase-locked loop circuit using a 1 MHz reference input. The phase-locked loop circuits produce an output frequency which is variable in 10 Hz steps from 65 to 95 MHz. The frequency of the synthesised 1st local oscillator is controlled digitally from Module 10J (the front-panel and control circuit module). The required frequency can be set using the front panel keypad or the manual tuning control, or from the memory, or by remote control.

3.2.3 The lower sideband of the mixer products is selected by a crystal band-pass filter, and passes to the 65 MHz 1st IF amplifier in Module 3D. This amplifier provides the input to the 2nd mixer.

3.3. 2nd IF Circuits

3.3.1 The inputs to the second mixer - Module 3D - are the 65 MHz 1st IF output and the 63.6 MHz second local oscillator input from the synthesiser in Module 9A. This local oscillator signal is generated by circuits similar to those used to generate the 1st local oscillator signal. The lower side-band of the 2nd mixer output is selected by one of a bank of five band-pass filters. All filters have a centre frequency of 1.4 MHz: they differ, however, in bandwidth and frequency offset as shown in Fig 1. These filters determine the bandwidth of the receiver, and are selected by the 'bandwidth' controls.

3.3.2 The 2nd mixer output is amplified in an a.g.c - controlled circuit in Module 4 and passes via a 4-way splitter to an A.M. filter, and three band-pass filters. Filter bandwidths are as follows:

LSB:	1.4 MHz	- 250 Hz
		- 3 kHz
USB:	1.4 MHz	+ 250 Hz
		+ 3 kHz
0.1:	1.4 MHz	± 50 Hz

3.3.3 The outputs from amplifiers A, B and D in Module 4 are fed to the detector and audio circuits in Module 5. The output from amplifier C is the pilot carrier input to the BFO circuit in Module 6.

3.4 A.G.C. Circuits

3.4.1 The input to the a.g.c detector can come from several sources. In USB mode it is taken via the USB filter. In LSB and P mode it is taken via the LSB filter. In ISB mode two inputs are connected, one from the LSB filter and one from the USB filter, this allows the a.g.c circuits to react to both sidebands. In all other operating modes it is taken from the output of the A.M. filter.

3.4.2 The output of the a.g.c. detector circuit is controlled in respect of rise and decay times by the time-constant and shaper circuits. The delay times are selected by the control functions of Module 10J. The rise time is tuned at approximately 5 ms, and decay time is selectable and can be 0.2, 2 or 10 seconds. The circuit will react to a short noise pulse on a substantially steady signal, the result will be a pulse rise time of about 5 ms and a decay time of about 50 ms. The a.g.c output is applied to the RF amplifier and to the 2nd IF amplifier. The manual RF - IF gain control operates via the a.g.c. circuits; it functions only when the a.g.c. is switched OFF.

3.5 Detector and Audio Circuits

3.5.1 The detector and audio circuits are in Module 5. They have three signal inputs and two BFO inputs, although not all are applied at any one time. The three signal inputs are derived from Module 4 outputs SKC, SKD and SKE. The two BFO inputs are supplied from Module 6; one is 1.5 MHz, while the other is a nominal 1.4 MHz, the precise frequency of which is controlled by the Mode setting, and can be.

a. 1.4 MHz exactly.

b. 1.4 MHz $\pm$ 8 kHz, the exact frequency being determined by the BFO control.

c. 1.4 MHz $\pm$ X, where the value of X is a preset, adjustable in steps of 100 Hz by switches in Module 6.

3.5.2 In Module 5, the first signal input is applied via SKA to the envelope detector, the second signal input is applied via SKB to product detector No 1, and the third signal input is applied via SKD to product detector No 2. Whichever input is active also drives product detector No 3: this uses the 1.5 MHz BFO input to produce the '100 kHz IF' receiver output.

3.5.3 The outputs of the envelope detector, and product detectors 1 and 2 pass to a switching circuit controlled by the MODE logic. The switching circuit outputs go to the three audio output stages.

a. The speaker and headphone amplifier.

b. Line output amplifier No 1.

c. Line output amplifier No 2.

3.5.4 The overall switching action can be seen in Table 2. Note that when ISB mode is selected, the output to the phones and speaker amplifier is selected by the position of the MONITOR USB - MONITOR LSB switch: this means that only one sideband of an ISB signal can be monitored.

TABLE 2 : DETECTOR SWITCHING

MODE	AMPLIFIER	DETECTOR	OUTPUTS
AM	A	Envelope	Speaker & phones, Line 1, Line 2
		Product 3	100 kHz IF
CW	B	Product 1	Speaker & phones
	C (to BFO)	Product 3	Line 1, Line 2 100 kHz IF
F	B	Product 1	Speaker & phones,
	C (to BFO)	Product 3	Line 1, Line 2 100 kHz IF
USB	B	Product 1	Speaker & phones,
		Product 3	Line 1, Line 2 100 kHz IF
LSB & P	D	Product 2	Speaker & phones,
		Product 3	Line 1, Line 2 100 kHz IF
ISB	A	Envelope	-
	B	Product 1	Speaker & phones, Line 1
	D	Product 2	Speaker & phones, Line 2
		Product 3	100 kHz IF

3.5.5 The four outputs are switched by the MODE and BANDWIDTH controls from Module 10J to four output lines as shown in Table 1.

TABLE 1 : 2ND I.F. OUTPUT SWITCHING

MODE	BANDWIDTH	ROUTE
A.M.	Not relevant	(a) via A.M. Filter to Amplifier A (b) via 0.1 Filter to Amplifier C
CW	Not 0.1	(a) via A.M. Filter to Amplifier B (b) via 0.1 Filter to Amplifier C
CW	0.1	(a) via 0.1 Filter to Amplifiers B and C
F	Not 0.1	(a) via A.M. Filter to Amplifier B (b) via 0.1 Filter to Amplifier C
LSB & P	-	(a) via LSB Filter to Amplifier D (b) via 0.1 Filter to Amplifier C
ISB	-	(a) via A.M. Filter to Amplifier A (b) via 0.1 Filter to Amplifier C (c) via LSB Filter to Amplifier D (d) via USB Filter to Amplifier B
USB	-	(a) via USB Filter to Amplifier B (b) via 0.1 Filter to Amplifier C

3.5.6 The manual volume control only affects the speaker and phones outputs. The line output amplifiers have independent preset output level controls.

3.6 BFO

3.6.1 Module 6 (BFO) contains the oscillators and associated control circuits, these generate the 1.5 MHz and 1.4 MHz (nominal) inputs for the detector circuits in Module 5. There are three oscillators. Oscillator 1 is permanently phase locked to the 1 MHz reference input from the external standard. Oscillator 2 can be locked to either the 1 MHz reference, the 1.4 MHz pilot carrier from amplifier C of Module 4, or the output from Oscillator 3. Oscillator 3 can be either phase-locked to the 1 MHz ref. or can be directly controlled by either the remote or local BFO control.

3.6.2 The output of Oscillator 1 is 1.5 MHz and goes to mixer 3 in Module 5. It is controlled by a phase-lock loop using a 50 kHz reference divided from the 1 MHz reference.

3.6.3 Oscillator 2 can be controlled by either of two phase detectors. With the receiver RE-INSERTED CARRIER control set to XTAL, the oscillator is controlled by the upper of the two phase detectors shown on the block diagram for Module 6. The reference input to this detector is one of two signals, depending on the receiver operating mode. If the mode is CW or F the reference input is the output of oscillator 3. Otherwise the reference input is a 100 kHz signal divided down from the 1 MHz reference, and an exact 1.4 MHz output is obtained.

3.6.4 The frequency of oscillator 3 can be controlled in two ways, depending on whether the receiver mode is CW or F. In the F mode, oscillator 3 is connected in a phase-lock using a 100 kHz reference input, and an output frequency of 100 kHz ± X is produced, where X is (8 kHz max) set in steps of 100 Hz by the offset switching: Oscillator 2 then produces an output frequency of 1.4 MHz ± X. In the CW mode, Oscillator 3 is directly controlled by either the remote, or local BFO control, and can be continuously varied 100 ± 8 kHz: Oscillator 2 then produces an output frequency of 1.4 MHz ± 8 kHz.

3.6.5 With the receiver RE-INSERTED CARRIER control set to RECON, oscillator 2 is controlled by the lower of the two phase detectors in the block diagram of Module 6. The reference input to this detector is the 1.4 MHz pilot carrier output from amplifier C of Module 4, oscillator 2 then produces an output of 1.4 MHz ± any variation in the frequency of the pilot carrier. Under these conditions a monitor phase-detector, compares oscillator 2 output frequency with the pilot carrier frequency, this produces a ZERO BEAT indication for use on the front-panel monitor meter.

3.7. Control

3.7.1 The control circuits are in Module 10J. 'Module 10' embraces the front panel and the circuit board mounted upon it. These items embody all the operator controls and logic functions of the receiver. The control function operates in conjunction with memory circuits in Module 12A, which also allows remote control of the receiver.

3.7.2 PR 2250G Control

The control functions of Module 10J give full manual control. There are six main control functions.

a. Frequency (tuning) control.

b. Local-remote control.

c. Mode control.

d. Bandwidth control.

e. AGC control.

f. Memory control.

3.7.2.1 The receiver can be continuously tuned between 10 kHz and 29.99999 MHz by:

a. entering the desired frequency on a keypad, or

b. the manual tuning knob.

In either case, the frequency is shown on a 7 segment LED display. The minimum frequency step is 10 Hz. Tuning controls the filter in Module 1 and the 1st local oscillator frequency. The frequency data is continuously applied to the memory interface and can be stored whenever desired. Similarly, stored frequency data is continuously available at the memory interface, and may be used to set the tuning logic whenever desired.

3.7.2.2 Local-Remote Control

Local and remote push-button controls are fitted. When in 'local', the front-panel controls only are operative. When in 'remote', control can only be exercised via the remote interface of Module 12A.

3.7.2.3 Mode and Bandwidth Control

3.7.2.4 Mode and bandwidth controls are interdependent in that selecting some modes automatically selects an appropriate bandwidth. However, where this is so, the automatically-selected bandwidth can be over-ridden if desired. The Mode function controls the BFO, the 2nd IF switching, and the detector switching (Modules 6, 4 and 5 respectively), and enables the reception of any one of seven types of signal, namely:

a. AM
b. CW
c. FSK (In 'F' or 'FIXED BFO OFFSET' mode)
d. USB
e. LSB
f. ISB
g. P

3.7.2.5 The Bandwidth control selects the 2nd IF bandwidth from one of five filter bandwidths:

a. 0.3 kHz Piccolo
b. 8 kHz
c. 1.2 kHz
d. 0.3 kHz
e. 0.1 kHz

3.7.2.6 AGC Control

The AGC keys select either the desired a.g.c decay time-constant (Module 4), or switch the a.g.c. off. The decay time constant can be selected from:

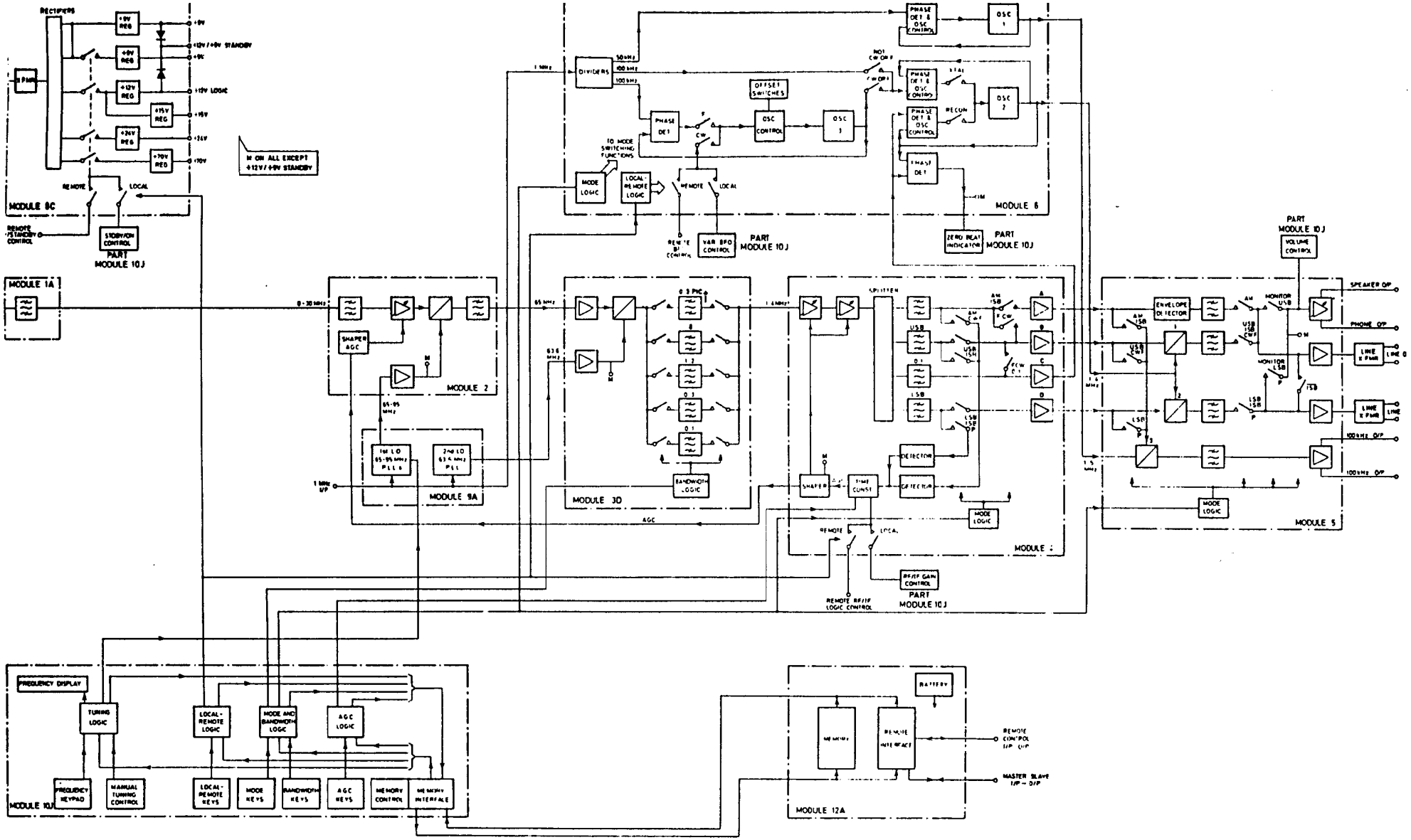
a. 10 sec.
b. 2 sec.
c. 0.2 sec.

Control is exercised on the a.g.c. circuit in Module 4.

3.7.2.7 Memory Control

The memory in Module 12A has sixteen channels. The front panel channel selector allows any one of these to be selected. All the control settings for any particular operating condition

can be stored in one of the memory channels and when required, recalled to control the receiver.



PR2250G

PR2250G functional block diagram

Fig 1

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3.8 Monitor Facilities

3.8.1 The receiver carries a monitor meter and associated selector switch. The signal monitor points are:-

a. 1st L.O. output level (LO1)

b. 2nd L.O. output level (LO2)

c. A G C Level (RF)

d. Audio line output level (AF)

e. Zero beat

f. D.C. Supplies

3.9 Power Supplies

3.9.1 The power supplies are contained in Module 8C. The receiver is powered from a single-phase a.c. supply of any frequency between 45 and 450 Hz. Voltage can be either between 100 and 125 V or between 200 and 250 V. Power consumption is 90VA. Either one of two power states can exist after the a.c. supply is connected: these are STANDBY and OPERATE. In standby certain circuits (such as the memory) are powered. All d.c. outputs are fully regulated and protected.

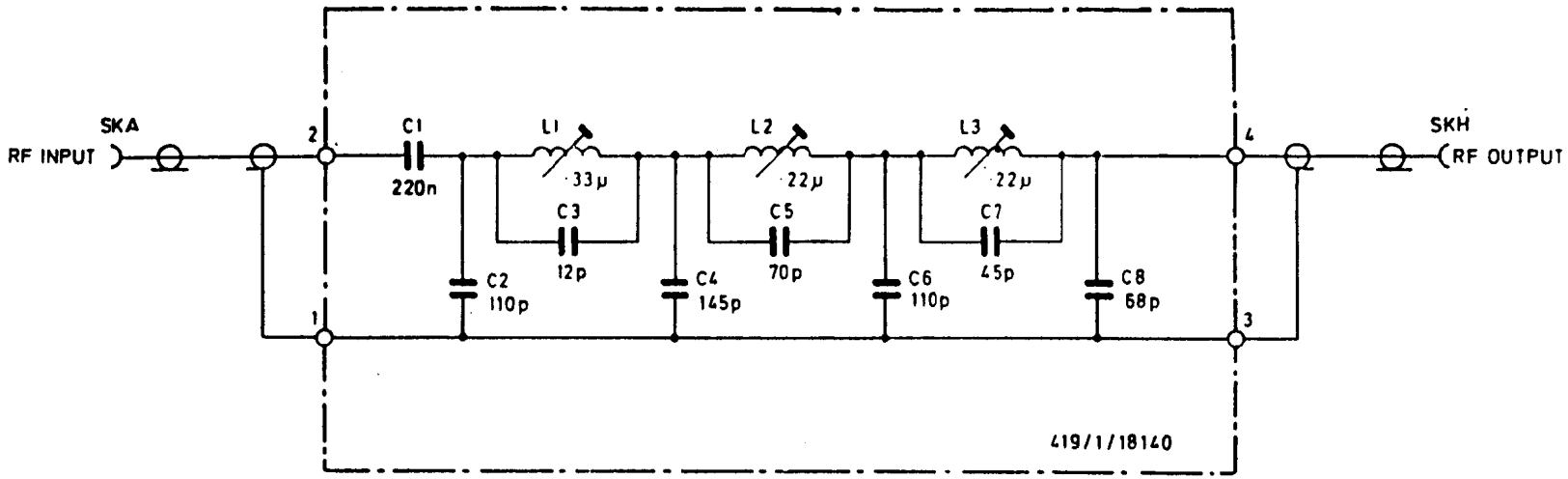
4. MODULE 1A : RF FILTER

4.1. Functional Description

Module 1A contains the 30 MHz low pass RF filter via which the antenna input is applied to the RF amplifier in Module 2.

4.2 Circuit Description

The antenna signal is applied via SKA to a low pass filter formed by L1, L2 and L3 together with associated capacitors. The output of this filter is connected directly to SKH.



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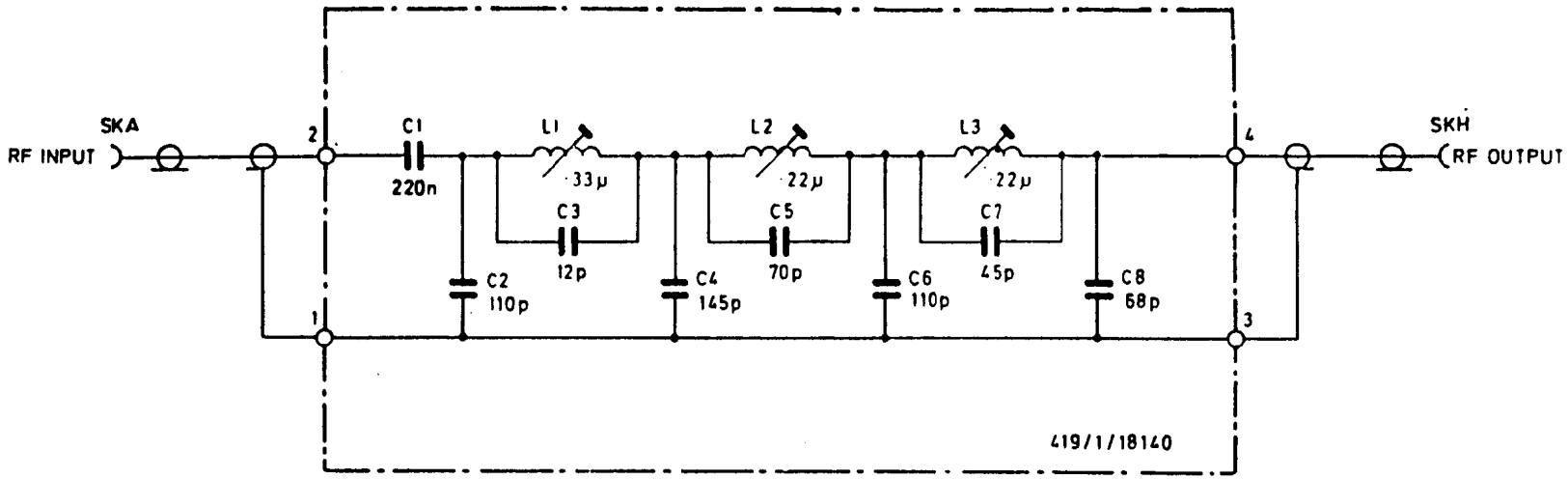
Module 1a circuit diagram

Fig. 1



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Module 1a circuit diagram

Fig. 1

5. MODULE 2 : RF AMPLIFIER/1ST MIXER

5.1 The filtered RF output from Module 1A is applied via SKA to a 0 - 30 MHz low-pass filter and thence to an a.g.c - controlled attenuator. A d.c. input controls the a.g.c shaper circuit, this reduces the control sensitivity with increase of signal strength. The amplitude-controlled RF signal is applied via the broad-band amplifier to the mixer. The local oscillator input frequency (65 MHz above the displayed frequency) is set by the receiver tuning controls. The difference frequency is extracted by a band-pass filter, giving the 65 MHz IF output.

5.2 AGC Shaper

The a.g.c. shaper circuit is made up of TR1, IC1 and associated components. The emitter-follower TR1 provides the d.c. input to the shaper operational amplifier IC1.

5.3 RF Amplifier

The a.g.c. controlled RF signal is applied via the transmission-line transformers T1 - T2 - T16 to a complementary pair push-pull RF amplifier, (TR5, TR6, TR7 and TR8).

5.4 Local Oscillator Amplifier

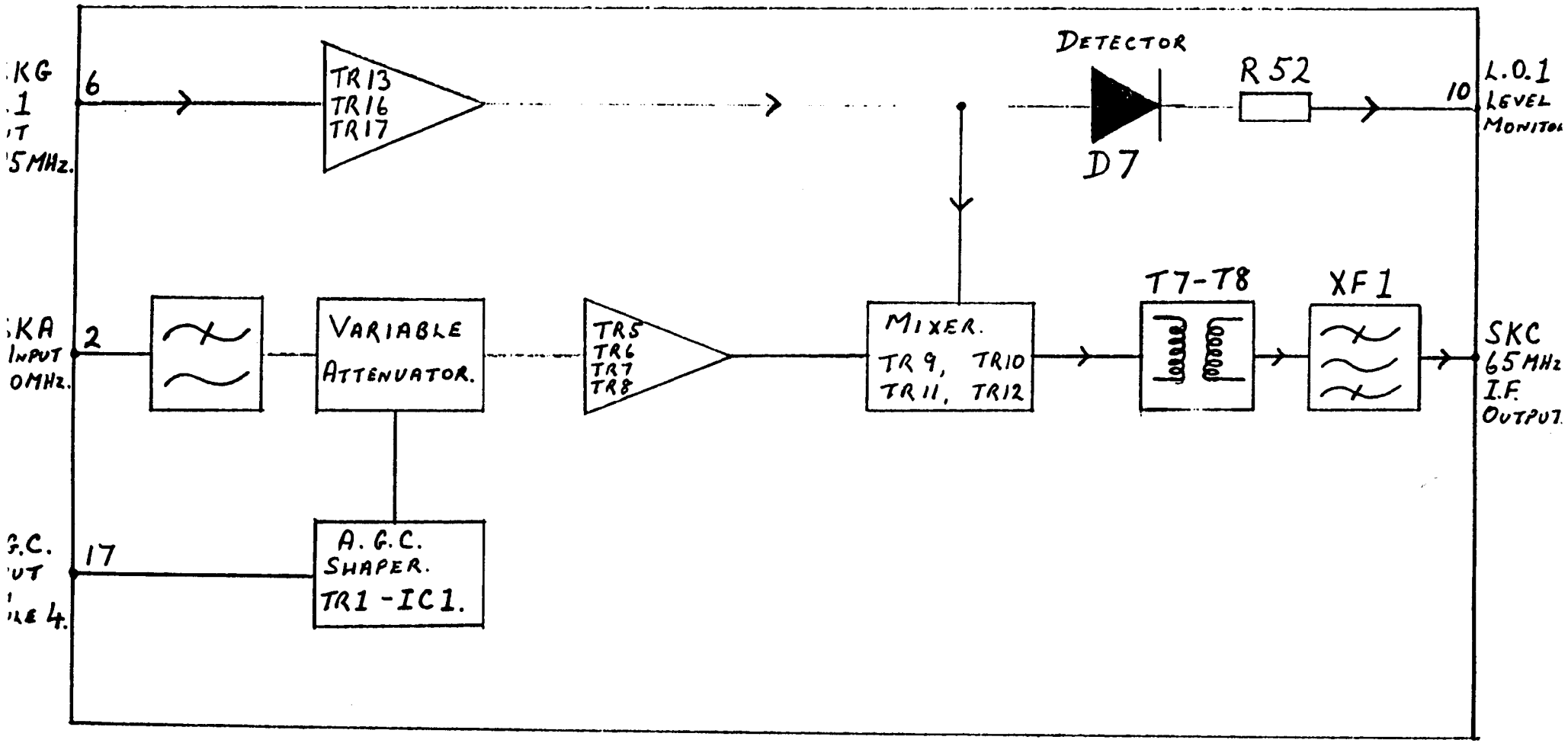
The 1st local oscillator input (65 - 95 MHz) is applied to common-emitter amplifier TR13. The output from TR13 is fed to TR16 and TR17 bases. TR16 and TR17 form a push-pull amplifier having transformer T15 as collector load. The signal output is fed via capacitors C52 and C53 to the input winding of T9 as the local oscillator input to the mixer.

5.5 Mixer

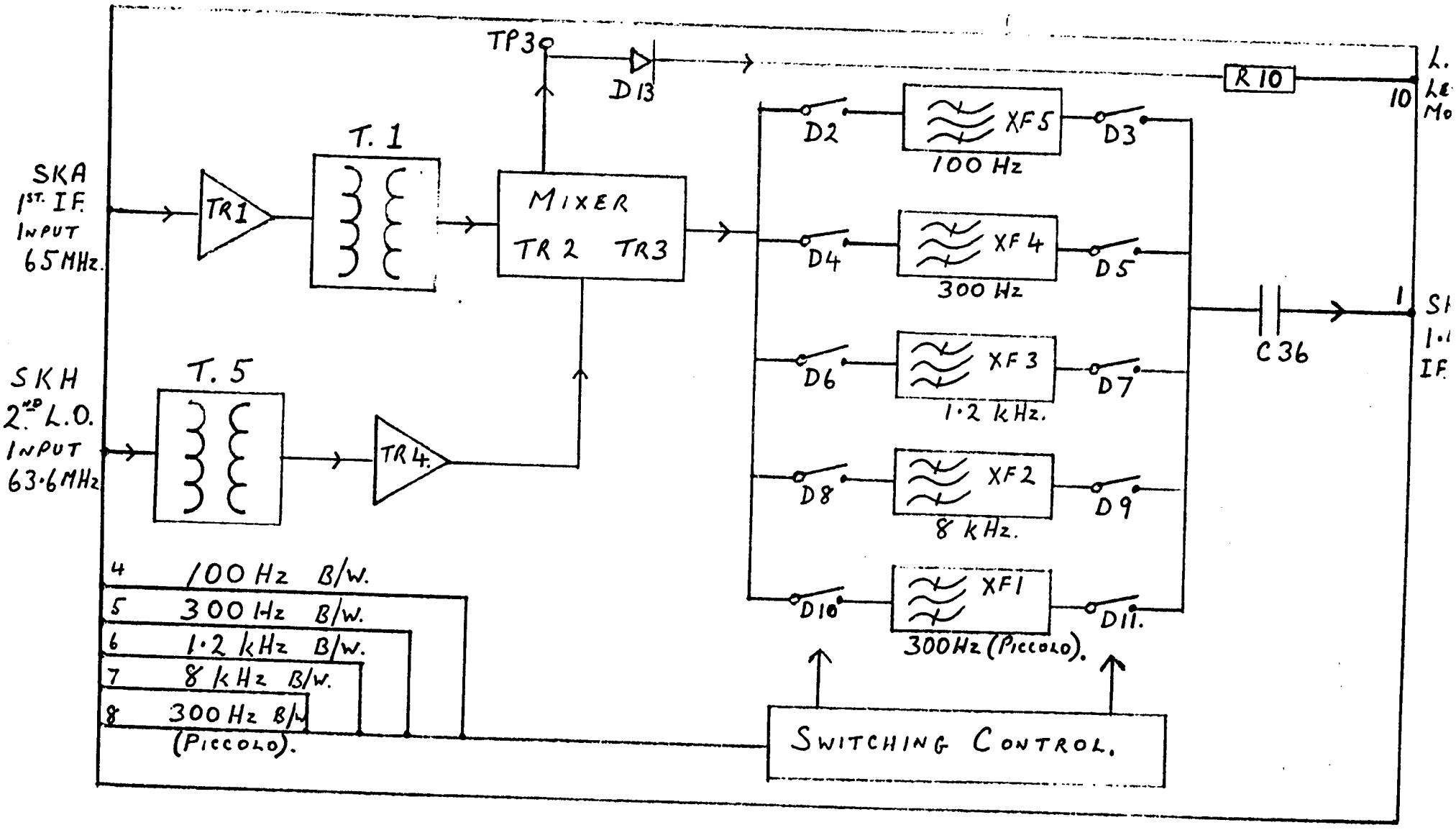
The mixer circuit formed by TR9, TR10, TR11 and TR12 is essentially a ring modulator formed by four field-effect transistors, with the inputs and outputs fed via balancing transformers. The output of the circuit is taken from the TR9 - TR12 junction and from the TR10 - TR11 junction. These two points produce antiphase signals

which are applied via T8 and T7 to the encapsulated 65 MHz crystal band-pass IF filter XF1. A low-pass filter is inserted in series with the output to provide additional high frequency attenuation. The output of the low-pass filter is applied to SKC as the 1st IF output signal.

5.6 A proportion of the local oscillator signal is rectified by D7, and appears on edge - pin 10, via R52 as a monitor output.



MODULE 2: R.F. AMPLIFIER & 1ST MIXER.



MODULE 3D: 1ST IF AMP 2ND MIXER & 2ND IF FILTERS.

6. MODULE 3D : 1ST IF AMPLIFIER, 2ND MIXER AND 2ND IF FILTERS

6.1 Functional Description

6.1.1 Module 3D contains the 1st IF amplifier, the second mixer and five selectable IF bandwidth filters.

6.1.2 The 65 MHz 1st IF signal, and the 63.6 MHz 2nd L.O. input, are amplified and fed to the mixer circuit. The 1.4 MHz difference frequency output is selected by one of a bank of five 1.4 MHz centre frequency filters. The selection of a particular filter is dependent upon the setting of the front-panel MODE and BANDWIDTH controls.

6.2 Circuit Description

6.2.1 1st IF Amplifier

The 1st IF amplifier is formed by TR1 and associated components. The 65 MHz output from Module 2 is applied via SKA to a crystal filter feeding the base of TR1. The collector-load transformer T1, matches the output to the load presented by the mixer (TR2 - TR3).

6.2.2 Local Oscillator Amplifier

The 63.6 MHz 2nd local oscillator output from the synthesiser (Module 9A) is applied via SKH to a series tuned circuit formed by C24 and L9. Transformer T5 matches the input signal to the load of TR4; L8 and C20 form an output parallel circuit tuned to 63.6 MHz.

6.2.3 2nd Mixer

6.2.3.1 TR2, TR3 and associated components form the mixer circuit. TR2 and TR3 are switched alternately by the local oscillator input, while

the drain/source voltage is provided by the signal input. The impedances in series with the transistors form loads across which the output signal is developed. Transformer T4 matches the signal to the load presented by the selected IF filter circuit.

6.2.3.2 The level of local oscillator drive to the mixer can be monitored on the front-panel meter. The drive to the base of TR2 is fed via R7 to D13 and associated components, and provides a d.c. current on edge connector-pin 10, which is proportional to drive level: this d.c. level is fed to the metering circuits.

6.2.4 2nd IF Filters

6.2.4.1 The difference frequency component in the output from the mixer is selected by one of five crystal filters.

XF1 : 1.4 MHz +360 Hz to +660 Hz

XF2 : 1.4 MHz ± 4 kHz

XF3 : 1.4 MHz ± 600 Hz

XF4 : 1.4 MHz ± 150 Hz

XF5 : 1.4 MHz ± 50 Hz

The filters are separate encapsulated units, wired to numbered terminal pins on the printed-circuit panel.

6.2.4.2 The inputs of all filters are paralleled via PIN diodes D2, D4 D6, D8 and D10. The outputs are paralleled via PIN diodes D3, D5, D7, D9 and D11. Each pair of diodes is switched on or off by the logic level applied to the base of the associated switching transistor. For example, D2 and D3 are controlled by the level applied to TR5 base.

6.2.4.3 At any time, one of switching transistors TR5 - TR9 has a +12V (logic 1) level applied to its base, while the remainder are held at a nominal OV (logic '0'). The emitter of one switching transistor is therefore at +11.5V, while the bases of the remainder are at a nominal OV. The two PIN diodes controlled by the conducting transistor are therefore forward biased, so connecting the associated filter between the mixer output and SKB. The +11.5V emitter level of the one conducting transistor is fed via the two associated conducting PIN diodes to R19 and R16, the junction of which is connected to OV, by Zener diode D12. A +6.2V level is therefore always available to reverse-bias the remaining eight PIN diodes.

7. MODULE 4 : 2ND IF AMPLIFIER, A.G.C. CIRCUITS AND IF FILTERS

7.1. Functional Description

7.1.1 Module 4 contains the 1.4 MHz 2nd IF amplifier, the 2nd IF distribution circuits, and the a.g.c. detector and time-constant circuits.

7.1.2 The 1.4 MHz 2nd IF signal from Module 3 is amplified in an a.g.c. controlled circuit and applied to the parallel inputs of an AM filter and three band-pass filters. 1.4 MHz (- 250 Hz to - 3 kHz), 1.4 MHz (+ 3 kHz to + 250 Hz) and 1.4 MHz $\pm$ 50 Hz. Outputs from selected lines are switched by the MODE logic inputs to the flow output lines as follows:-

(1) AM Mode

a. From AM filter to SKC
b. From 100 Hz filter to SKF

(2) CW Mode (not 0.1 B/W)

a. From 100 Hz filter to SKF

(3) CW Mode and 0.1 B/W

a. From 100 Hz filter to SKD and SKF

(4) F Mode (not 0.1 B/W)

a. From AM filter to SKD
b. From 100 Hz filter to SKF

(5) F Mode and 0.1 B/W

a. From 100 Hz filter to SKD and SKF

(6) LSB and P Mode (not 0.1 B/W)

a. From LSB filter to SKE
b. From 100 Hz filter to SKF

(7) ISB Mode (not 0.1 B/W)

a. From AM filter to SKC
b. From 100 Hz filter to SKF
c. From LSB filter to SKE
d. From USB filter to SKD

(8) USB Mode (not 0.1 B/W)

a. From USB filter to SKD
b. From 100 Hz filter to SKF

7.1.3 In all operating modes except USB, ISB, LSB and Piccolo the a.g.c. detector input is connected to the IF output via the AM filter. In USB mode it is connected via the USB filter. In LSB and Piccolo mode it is connected via the LSB filter. In ISB mode, two inputs are connected, one from the LSB filter and one from the USB filter, in order that the a.g.c. circuits may react to both sidebands. The varying d.c. output produced by the a.g.c. detector is controlled in respect of rise and decay times by the time-constant circuits: the decay times can be selected by front-panel control.

7.2. Circuit Description

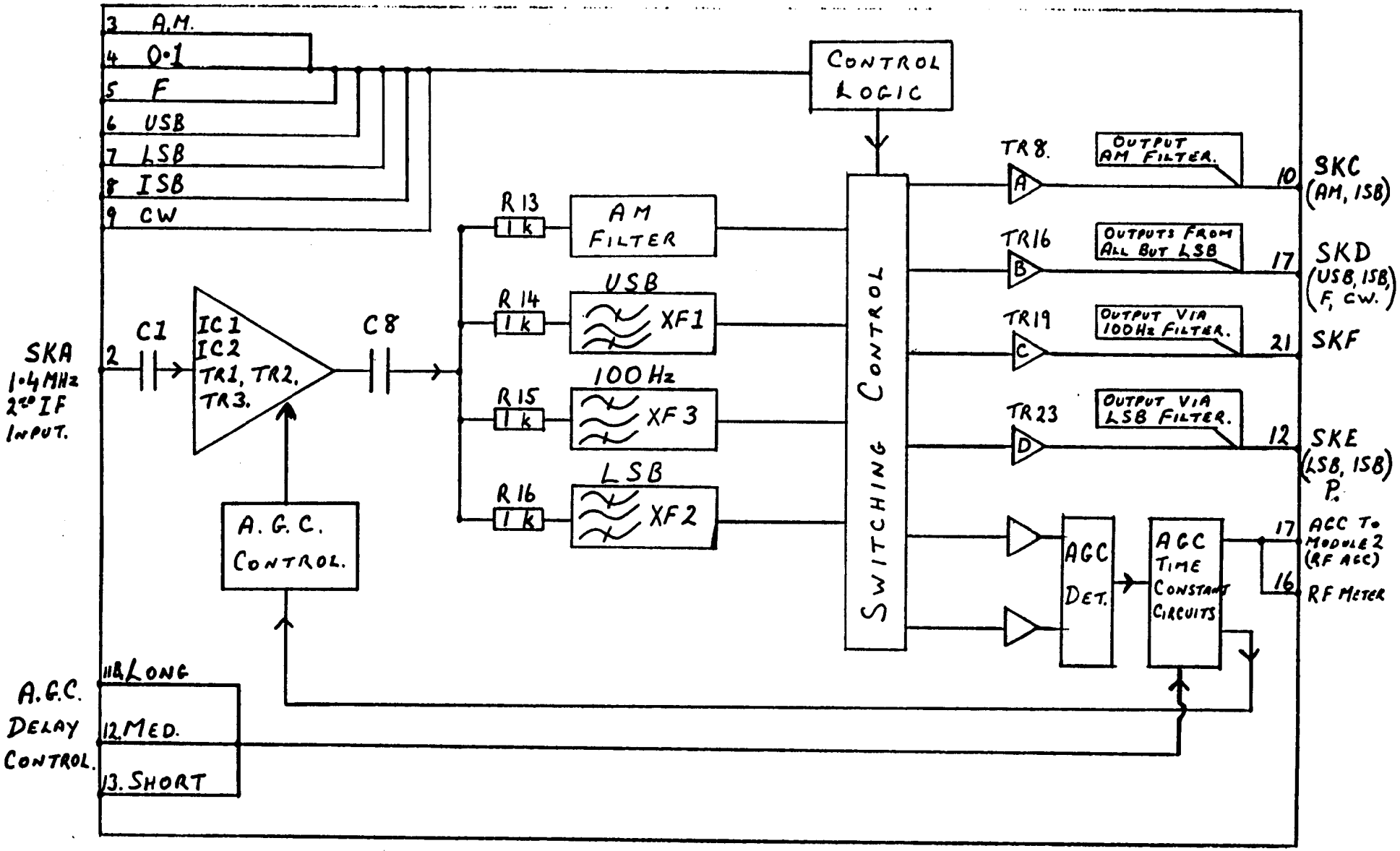
7.2.1 2nd IF Amplifier

7.2.2 The 1.4 MHz second IF amplifier is formed by IC1, IC2, TR1, TR2, TR3 and associated components. The input signal is applied from SKA via capacitor C1 to a two stage non-inverting amplifier formed by IC1 and IC2. The amplifier is a.g.c. controlled.

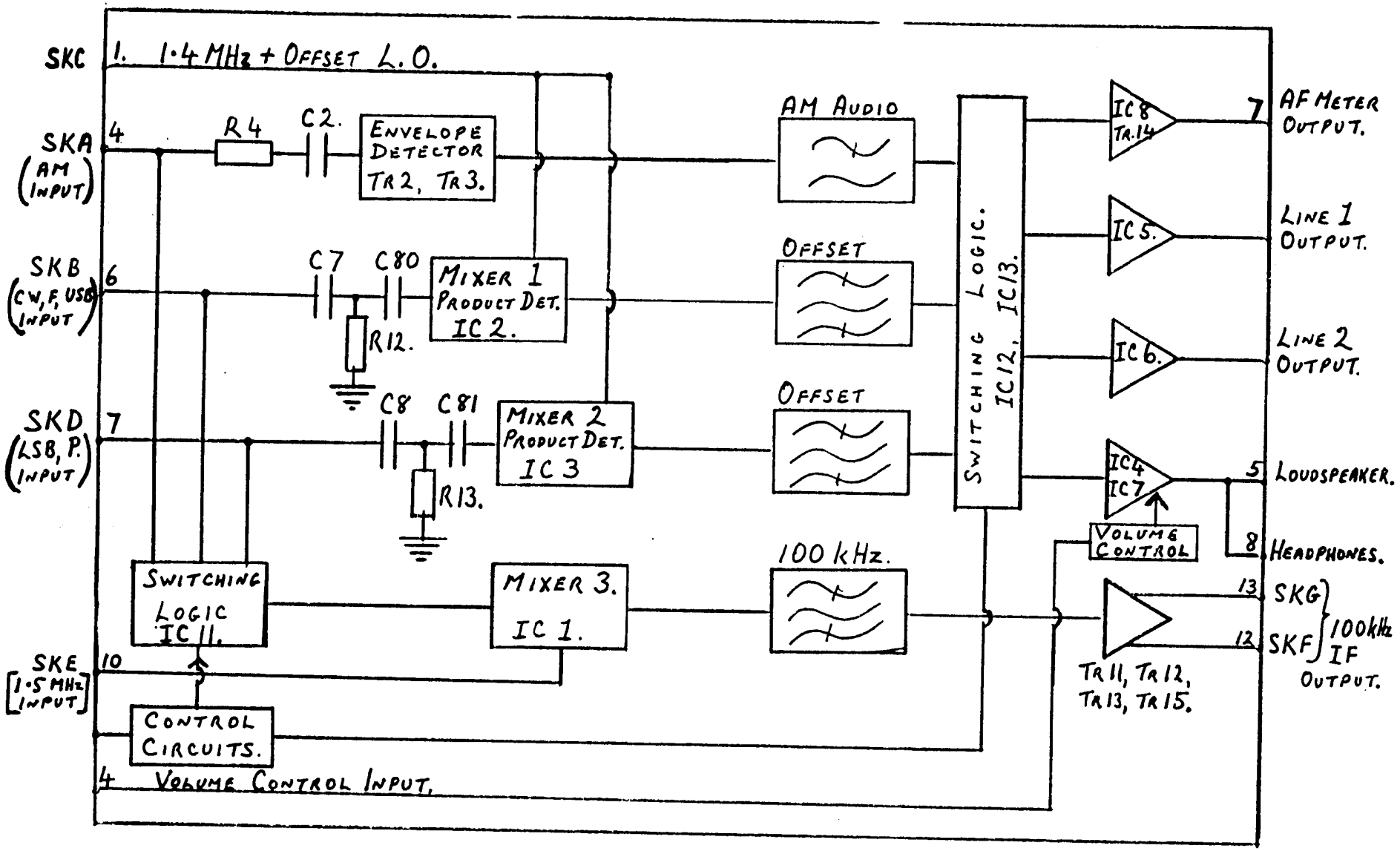
7.2.3 The output from IC2 is applied via emitter-follower TR1 to an inverting cascade stage formed by TR2, TR3 and associated components.

7.3. Bandpass Filters

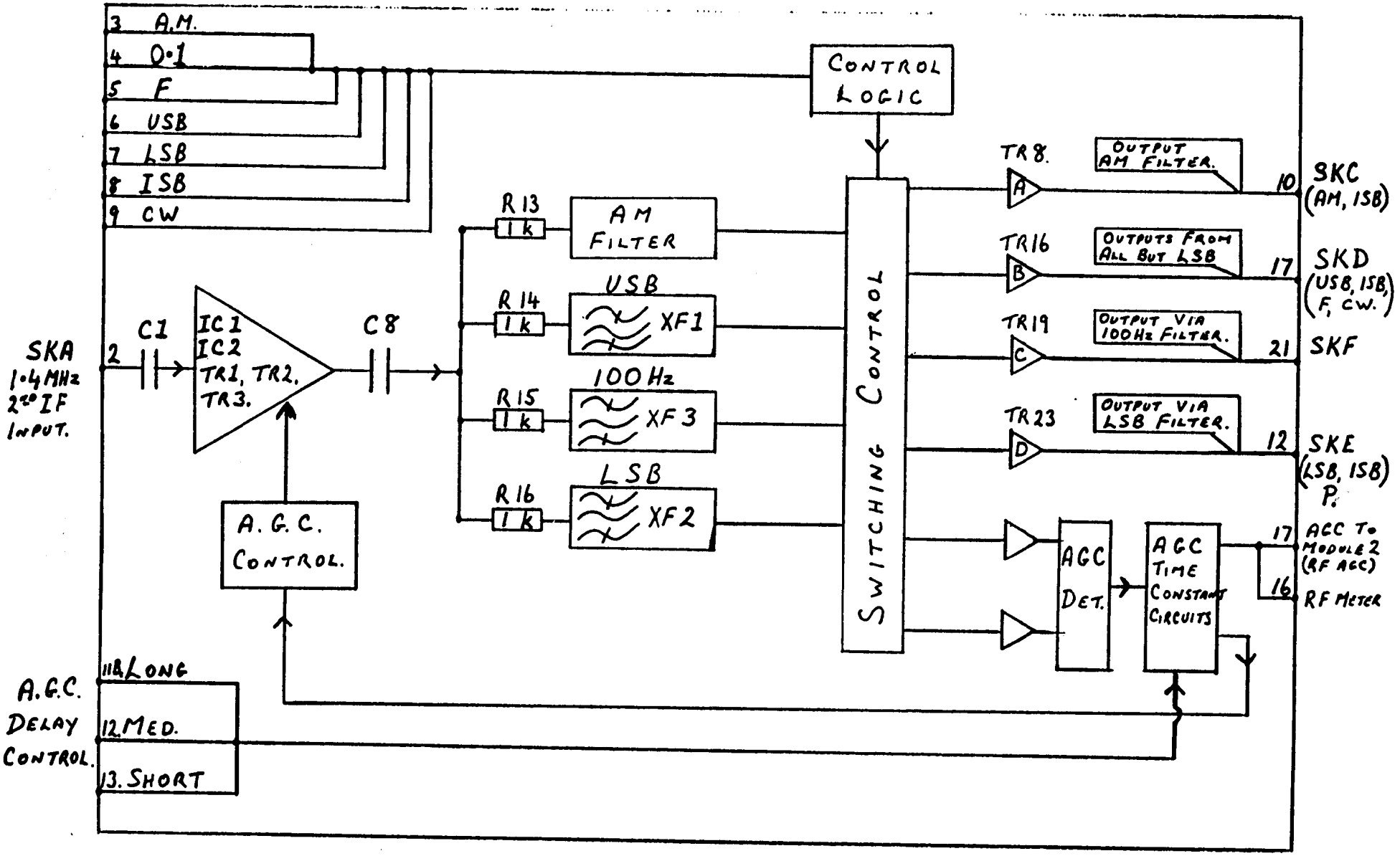
7.3.1 The 1.4 MHz amplified 2nd IF output from TR3 is applied via C8 to the parallel inputs of three bandpass filters and the AM filter. The output impedance from TR3 is very low. The characteristic input impedance of each filter is 1 kilohm, therefore the filter inputs are supplied via series resistors R13, R14, R15 and R16. XF1, XF2 and XF3 are encapsulated crystal filters. The 'AM filter' is formed by C11, C12, C13, C14, C15, L4 and L5. The output from each filter is taken via an emitter-follower buffer to the switching circuits. Sideband reversal occurs in Module 2 (output from the 65 MHz IF band-pass filter), and for this reason XF1 in the USB path is a lower sideband filter and XF2 in the LSB path is an upper sideband filter.



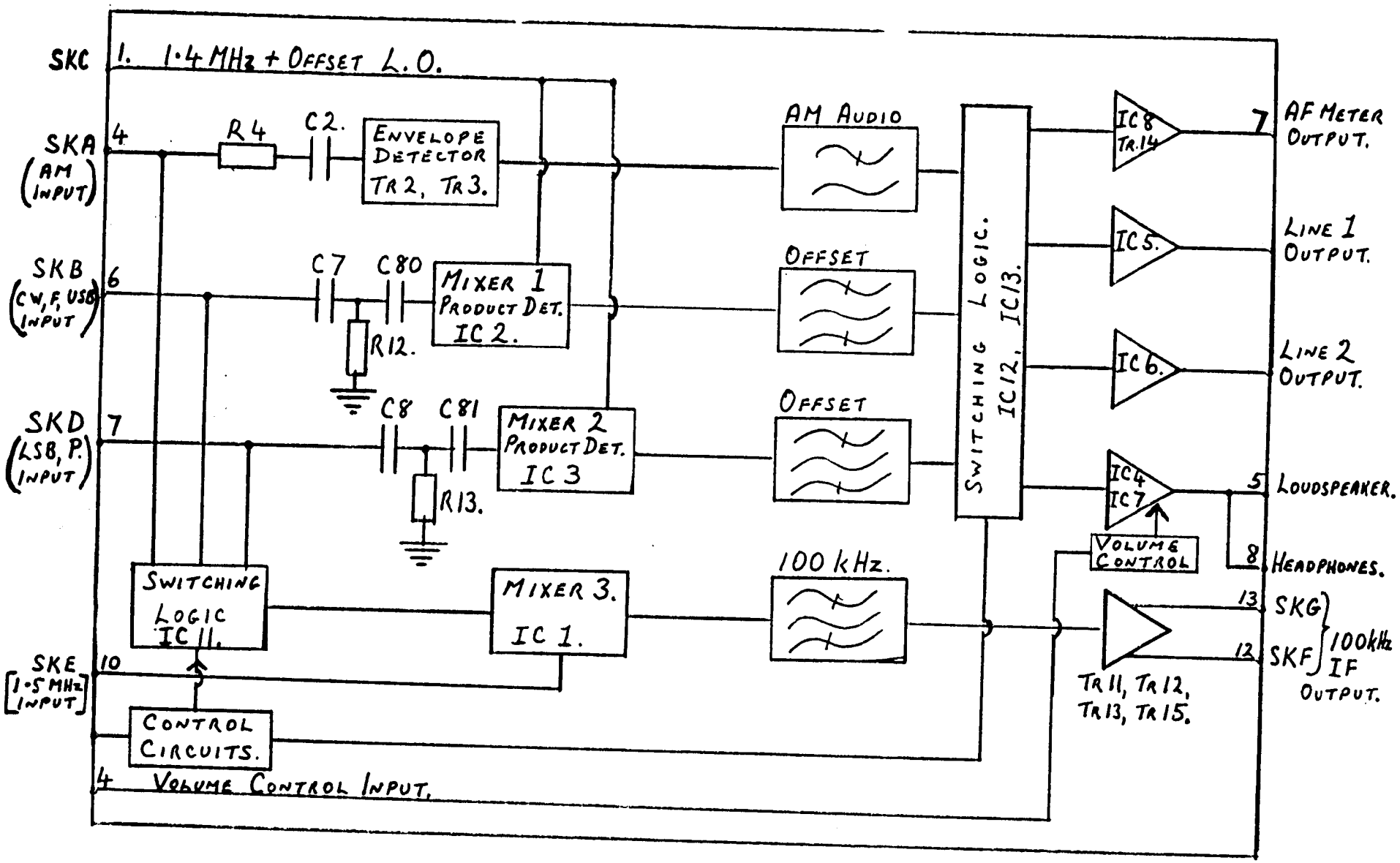
MODULE 4: 2ND IF AMP., A.G.C. & IF FILTERS.



Module 5: Detectors & Output Amplifiers.



MODULE 4: 2ND IF AMP., A.G.C. & IF FILTERS.



Module 5: Detectors & Output Amplifiers.

8. MODULE 5 : DETECTORS AND OUTPUT AMPLIFIERS

8.1 Functional Description

8.1.1 Module 5 contains the detector and output circuits of the receiver, together with the associated switching and control circuits.

8.1.2 The detection circuits consist of an envelope detector and three mixers. Two of these mixers function as product detectors; these two share a common 1.4 MHz + OFFSET, local oscillator input. The third mixer receives a 1.5 MHz local oscillator input. Three 1.4 MHz IF input signals from Module 4 are applied to Module 5. In ISB mode, two are present simultaneously: in all other modes, only one is present at any given time. The applied input (or inputs, ie both sidebands on ISB) is always connected to the input of the third mixer. As this mixer has a 1.5 MHz local oscillator, therefore, any signal input to Module 5 is always down-converted to 100 kHz to give the IF output.

8.1.3 An amplitude-modulated input signal applied to the envelope detector produces an audio output; this is used in the AM mode. An input signal applied to either product detector produces an output at whatever offset frequency has been set on the local oscillator; this is employed in all modes except AM. When working ISB, the incoming signal is split in Module 4: the upper sideband is fed to Mixer 1, and the lower sideband is fed to Mixer 2.

8.1.4 Three audio amplifiers and a meter amplifier are also present in the Module. One provides the phones and speaker outputs. The other two providing the two independent LINE outputs. The inputs to all three audio amplifiers are selected from the appropriate detectors by the switching logic controlled from Module 10J.

8.1.5 Except when working ISB, all detected signals are fed to all audio amplifiers. When working ISB, one line amplifier receives USB and the other receives LSB: the inputs to the meter amplifier and the phones and speaker amplifier are then either LSB or USB, determined by the setting of the front-panel MONITOR toggle switch.

8.2 Circuit Description

8.2.1 Detectors

8.2.1.1 Envelope Detector (Linear Detector)

The AM input from SKA is applied to the inverting amplifier stage formed by TR2 and TR3. The half-wave rectified output from D2 - R11 junction is fed via a 1.4 MHz rejector circuit and second-order low-pass active filter to output stage TR7.

8.2.1.2 Product Detectors

IC2 and IC3 are each double balanced modulators which function similarly to ring modulators but without the use of transformers. Each product detector output is taken via an amplifier stage and level presetting control and applied to a second-order, low-pass active filter. The filter outputs are fed to the transfer gate switching circuits. Since the IF inputs are 1.4 MHz and the local oscillator frequency is 1.4 MHz plus an offset determined in Module 6, then the outputs are at offset frequency.

8.2.1.3 100 kHz MIXER AND OUTPUT CIRCUIT

The 100 kHz mixer circuit of IC1 is identical with that of IC2 and IC3, except that the local oscillator frequency is 1.5 MHz. The output frequency is therefore 100 kHz, filtered by a passive band-pass circuit. The filtered 100 kHz output is amplified by TR11, 12, 13 and 15 to produce two unbalanced 50 ohm outputs, on SKG and SKF.

9. MODULE 6 : B F O

9.1 Basic Description

Module 6 contains the 1.4 MHz and 1.5 MHz oscillators and their associated control circuits, for the detector circuits in Module 5.

9.1.2 Oscillator 1 and oscillator 2 provide the two outputs from Module 6. Oscillator 1 is permanently phase-locked to the 1 MHz reference input. Oscillator 2 can be phase-locked to the 1 MHz input, the 1.4 MHz carrier input, or the output from Oscillator 3. Oscillator 3 can be locked to the 1 MHz reference input (in which case its frequency can be set in 100 Hz steps by the OFFSET switches) or controlled directly by the variable d.c. BFO input from the front-panel BFO control.

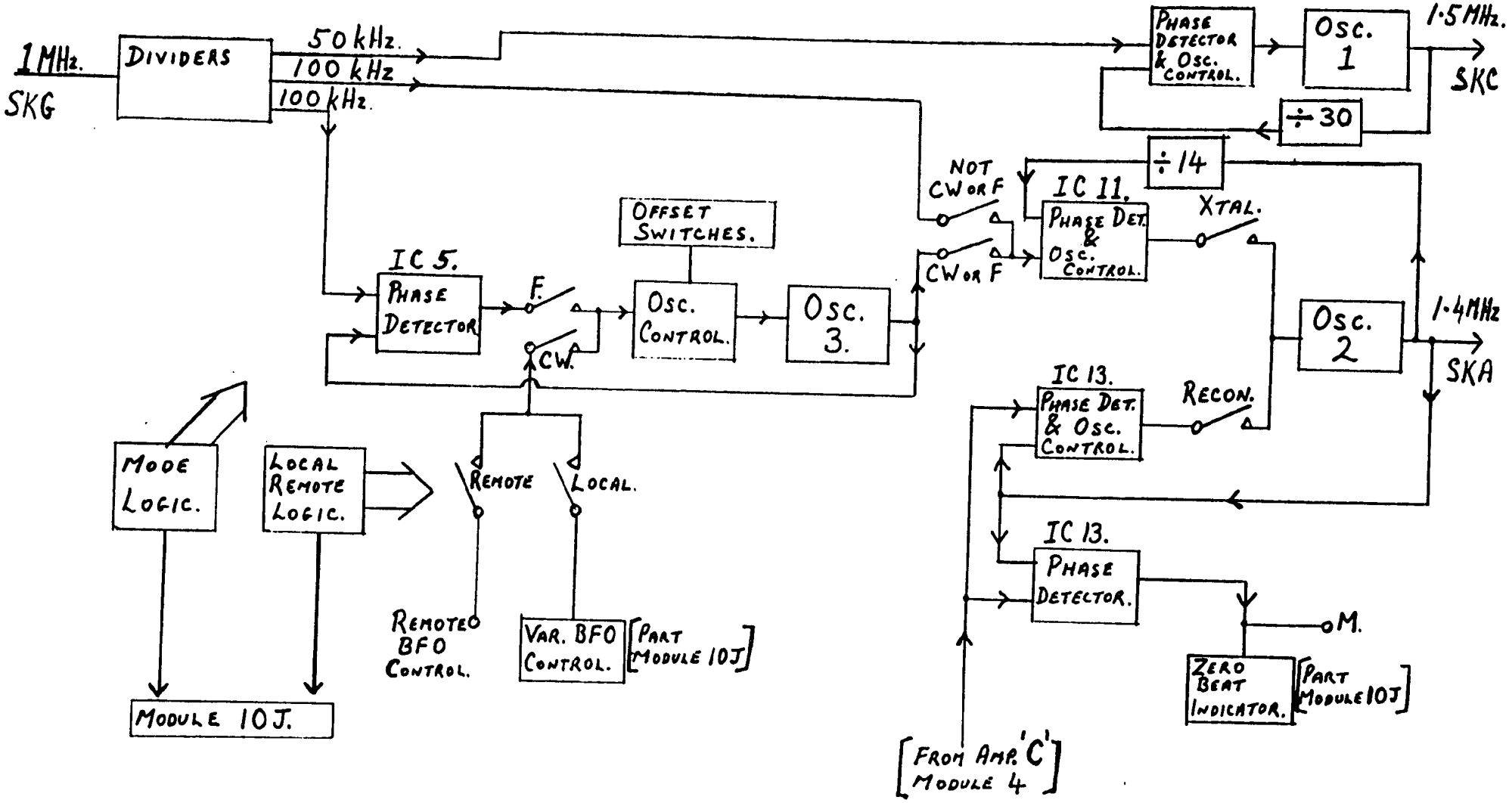
9.2 Functional Description

9.2.1 Oscillator 1

The frequency of Oscillator 1 is controlled by the output of a phase-detector with two 50 kHz inputs. One of these is the oscillator output taken via a division ratio of 30, and the other is the 1 MHz reference input taken via a division ratio of 20. The 1.5 MHz output from oscillator 1 is therefore phase-locked to the 1 MHz reference input.

9.2.2 Oscillator 2

Oscillator 2 is controlled by a selected phase-detector, either IC11 or IC13. When controlled by IC13, it is phase-locked to the 1.4 MHz carrier input (ie from amplifier 'C' in Module 4). When controlled by IC11, the output from oscillator 2 is fed back at 100 kHz via mixer IC17: control is exercised either by a 100 kHz reference derived from the 1 MHz reference, or by the output from oscillator 3.


1 MHz.
SKG
DIVIDERS
50 kHz.
100 kHz
100 kHz.
PHASE DETECTOR & OSC. CONTROL.
OSC. 1
1·5 MHz.
SKC
÷ 30
÷ 14
NOT CW OR F
IC 11.
PHASE DET. & OSC. CONTROL.
XTAL.
OFFSET SWITCHES.
IC 5.
PHASE DETECTOR
F.
CW.
OSC. CONTROL.
OSC. 3.
CW OR F
OSC. 2
1·4 MHz
SKA
IC 13.
PHASE DET. & OSC. CONTROL.
RECON.
MODE LOGIC.
LOCAL REMOTE LOGIC.
REMOTE
LOCAL.
IC 13.
PHASE DETECTOR.
M.
REMOTE BFO CONTROL.
VAR. BFO CONTROL.
[PART MODULE 10J]
ZERO BEAT INDICATOR.
[PART MODULE 10J]
MODULE 10J.
[FROM AMP. 'C' MODULE 4]

MODULE 6 : BFO

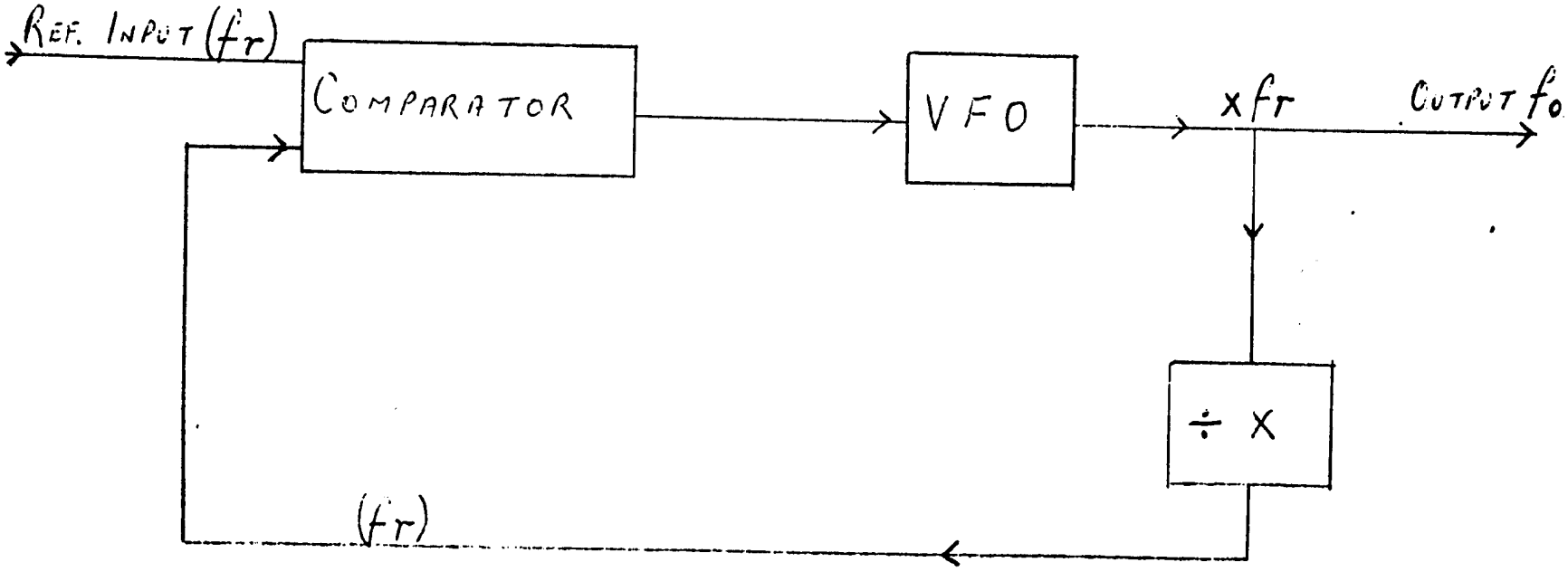


FIG (a) BASIC PHASE-LOCK LOOP

9.2.3 Oscillator 3

Oscillator 3 is controlled either by the output from phase-detector IC5 or by the variable d.c. BFO control input. When controlled by the output from IC5, it is phase-locked to 100 Hz derived from the 1 MHz reference. The oscillator output is applied to the phase detector via a division ratio which can be set by switches. As the reference input is 100 Hz (1 MHz ÷ 10,000), oscillator 3 will lock at whatever frequency produces a 100 Hz output from the variable divider (ie offset switches). The offset frequency produced in this way can be set in 100 Hz steps above and below the nominal 100 kHz frequency of oscillator 3. When directly controlled by the BFO control input, oscillator 3 does not form part of a phase-lock loop.

10. MODULE 9A : SYNTHESISER

10.1 Introduction

Module 9A contains two phase-lock loop controlled oscillator circuits. One produces the fixed-frequency (63.6 MHz) 2nd local oscillator output, while the other produces the variable-frequency (65 to 95 MHz) 1st local oscillator output; this output can be varied in steps of 10 Hz.

10.2 Basic Principles

The basic phase-lock loop circuit employed is of the form shown in figure (a). The VFO output frequency is X times the reference frequency, where X is the division ratio of the loop divider circuit. If this division ratio is variable, the output frequency is also variable. The output frequency variation step-size is equal to the reference frequency applied to the comparator and this limits the minimum step-size. If, for example a 10 Hz reference frequency were employed then the output frequency could be varied in 10 Hz steps. However, the time taken for the loop to 'lock' increases as the reference frequency decreases, so there is a limit to the fineness of the minimum output step from the circuit shown in Figure (a). A divider is frequently inserted in the REF INPUT line to produce a suitable reference input frequency to the comparator.

10.2.1 Consider the circuit shown in Figure (b), wherein a mixer and a variable divider precede the circuit of Figure (a). The upper side-band output from the mixer is applied to the 'reference' input of the comparator. In Figure (b), let reference 2 be of variable frequency. Also, let both variable dividers at all times produce identical division ratios.

10.2.2 If both dividers in Figure (b) have a division ratio of X, then the final output frequency (fo) is X times the USB filter output frequency. The USB filter output frequency is:-

$$\text{REF 1} + \frac{\text{REF 2}}{X}$$

Therefore, the final output frequency fo is

$$X(\text{REF 1} + \frac{\text{REF 2}}{X})$$

or

$$X.\text{REF 1} + \text{REF 2}$$

and can be varied in two ways. Either term X (the divider ratio) or REF 2 frequency can be varied to change the value of fo.

This action is illustrated as follows:-

(i) REF 1 = 1 MHz; REF 2 = 1.1 MHz; X = 50; fo = 50 $(1 + \frac{1.1}{50}) = \underline{51.1 \text{ MHz}}$

(ii) REF 1 = 1 MHz; REF 2 = 1.2 MHz; X = 50; fo = 50 $(1 + \frac{1.2}{50}) = \underline{51.2 \text{ MHz}}$

(iii) REF 1 = 1 MHz; REF 2 = 1.1 MHz; X = 76; fo = 76 $(1 + \frac{1.1}{76}) = \underline{77.1 \text{ MHz}}$

ie fo = X + REF 2 where REF 1 = 1 MHz

10.2.3 If the circuit shown in Figure (b) is further modified by the inclusion of a divide-by-ten circuit between the USB filter output and the comparator input, then the output frequency is given by fo = 0.1 (X + REF 2) where REF 1 = 1 MHz. This arrangement can be used in a cascade loop as shown in Figure (c). The first stage is as shown in Figure (a); the second and third are as shown in Figure (b) with the divide-by-ten modification, and the fourth stage is as shown in Figure (b).

10.2.4 If terms W, X, Y and Z of Figure (c) are given values of W = 40, X = 50, Y = 60 and Z = 70, then the frequencies at points A, B, C, and D in Figure (c) are as follows:-

A = (W x REF 1) = 40 x 1 = 40 MHz
B = 0.1(X+A) = 0.1(50+40) = 9 MHz
C = 0.1(Y+B) = 0.1(60+9) = 6.9 MHz
D = (Z+C) = (70+6.9) = 76.9 MHz

10.2.5 Table 1 shows the effect of varying terms W, X,Y and Z separately. By this method, four division ratio controls (one for each stage) can be calibrated in terms of digits of the output frequency fo. These controls can be further combined by external circuits into one single rotary knob.

TABLE 1 : VARIATIONS OF DIVIDER TERMS

Divider Term				Varied by	Varied by	Varied by	Varied by
W	X	Y	Z	Term Z	Term Y	Term X	Term W
40	50	60	70	7 6	. 9	0	0 MHz
40	50	60	80	8 6	. 9	0	0 MHz
40	50	60	71	7 7	. 9	0	0 MHz
40	50	60	70	7 7	. 0	0	0 MHz
40	51	60	70	7 6	. 9	1	0 MHz
40.5	50	60	70	7 6	. 9	0	5 MHz

10.2.6 The range of variation of term Z is decided by the desired frequency range. The variations of terms Y and X are both over a range of ten. In the example given, the variation of term W is over a range of one in steps of 0.1 or less: in a practical circuit, term W is a division ratio of hundreds and therefore would vary over a larger range. The smallest step by which output frequency can be varied, so producing a circuit (Figure (c)) in which fine variations of frequency can be made, without incurring the penalty of long 'lock' time.

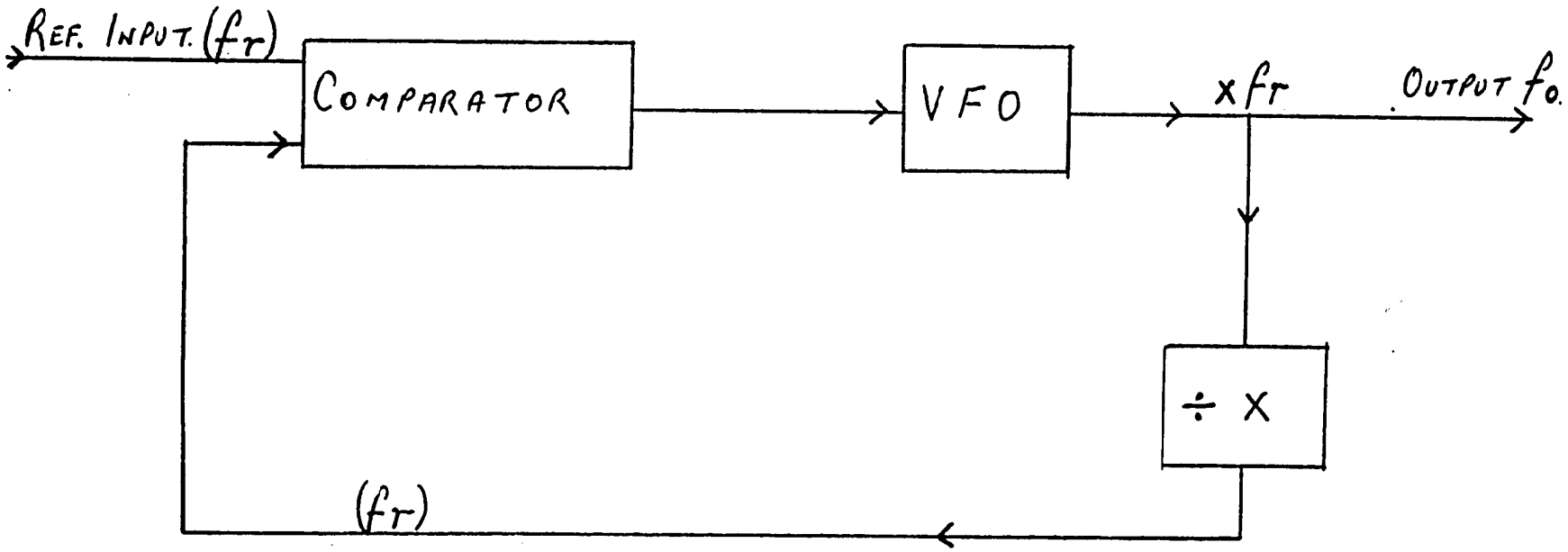


FIG. (a) BASIC PHASE-LOCK LOOP

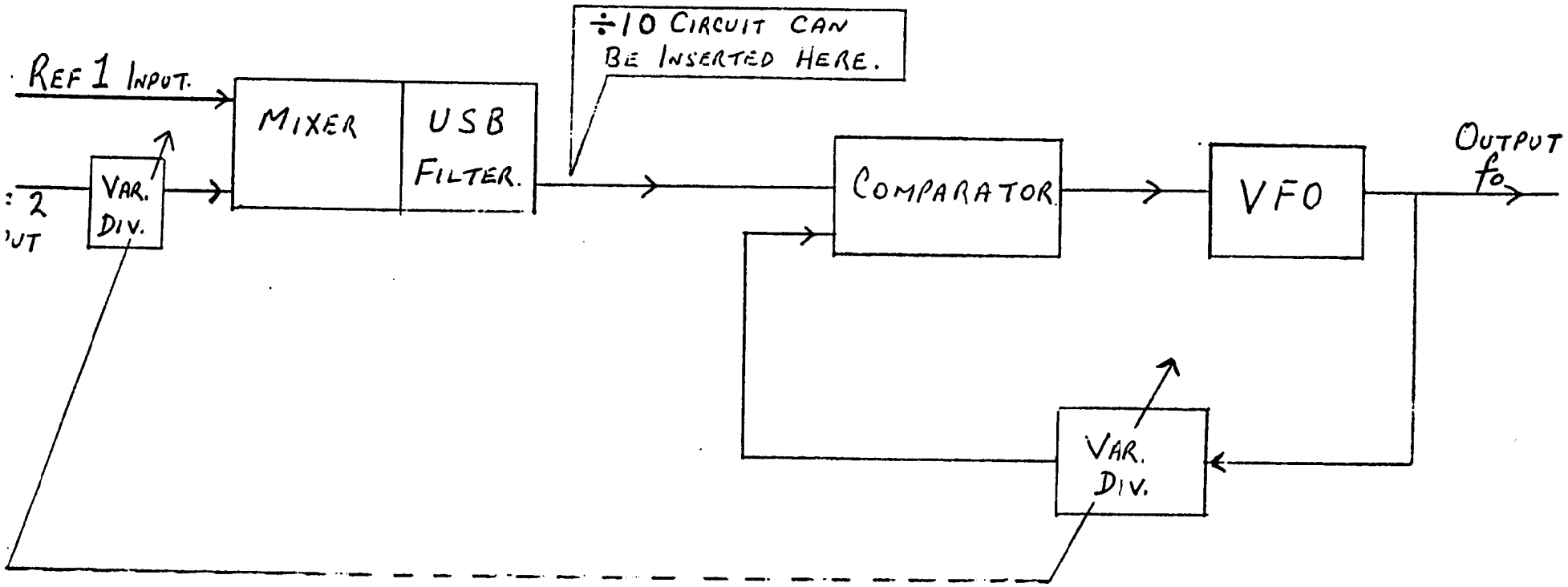


Fig (b) Development of Fig (a) Circuit.

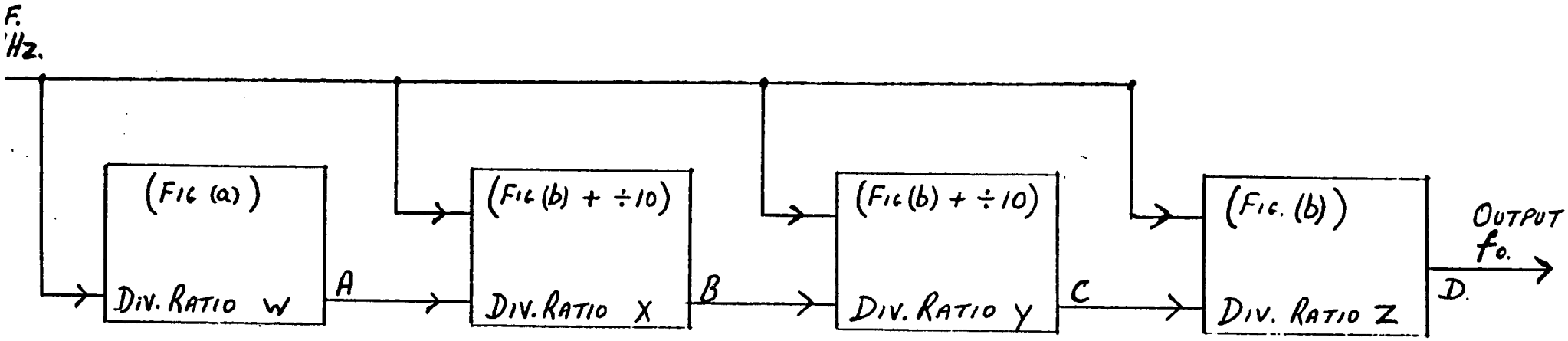
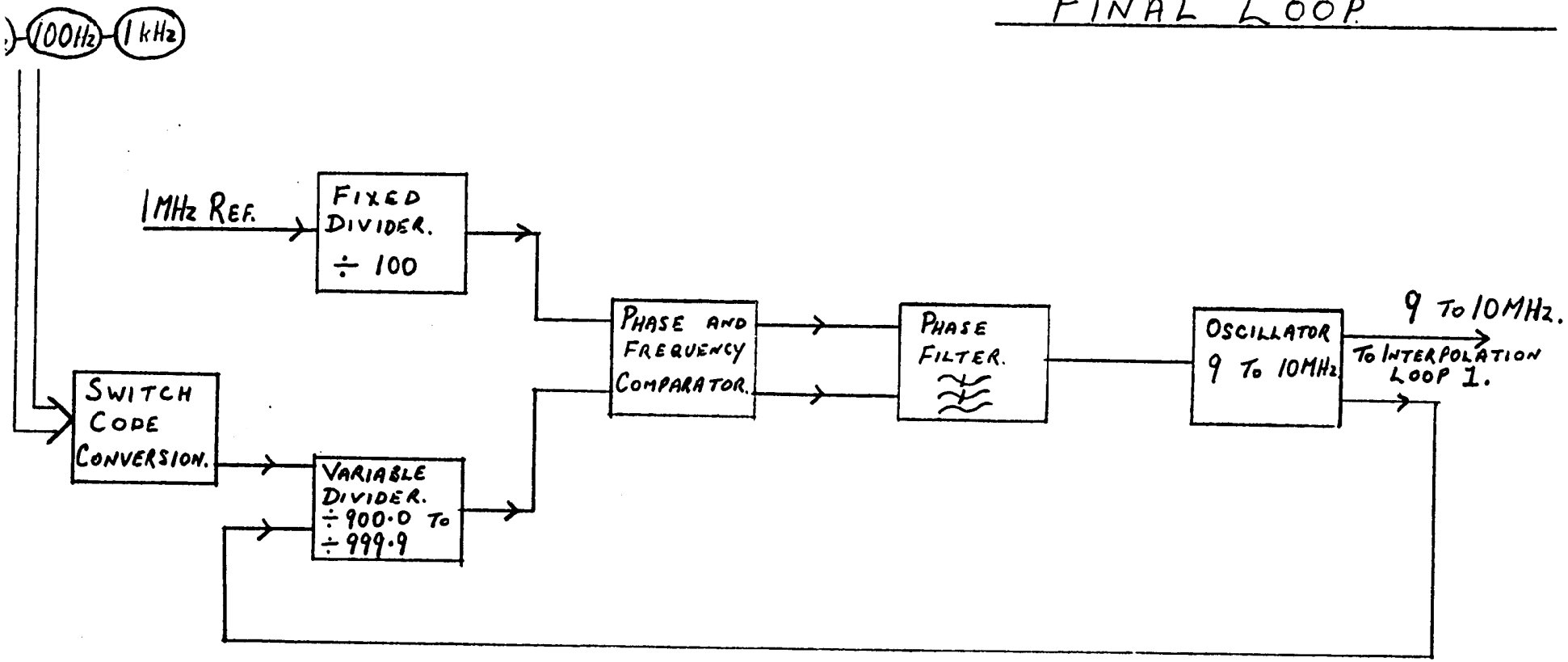


FIG. (C) FOUR - TERM CASCADE PHASE-LOCK LOOP.

FINAL LOOP



MODULE 9A: SYNTHESISER.

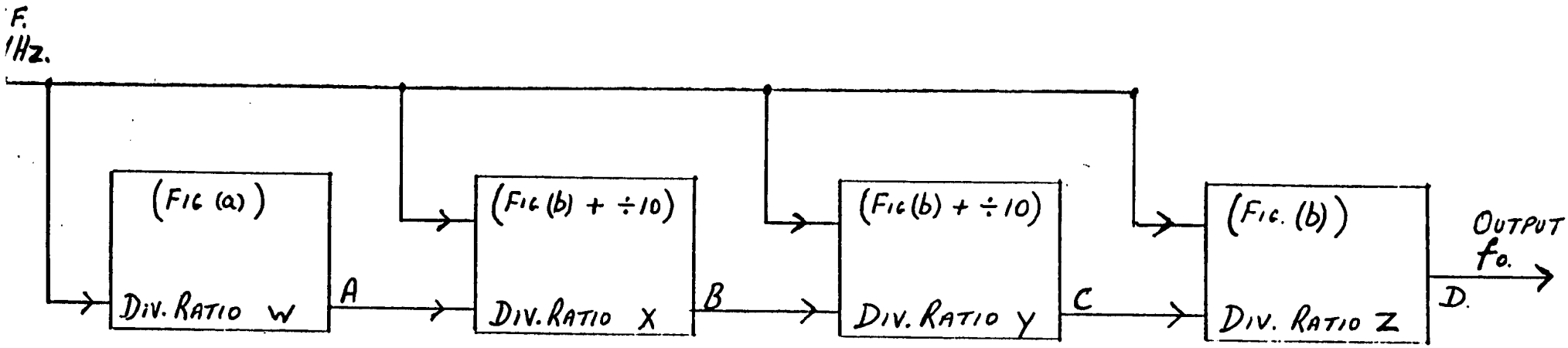


Fig. (c) Four - Term Cascade Phase-Lock Loop.

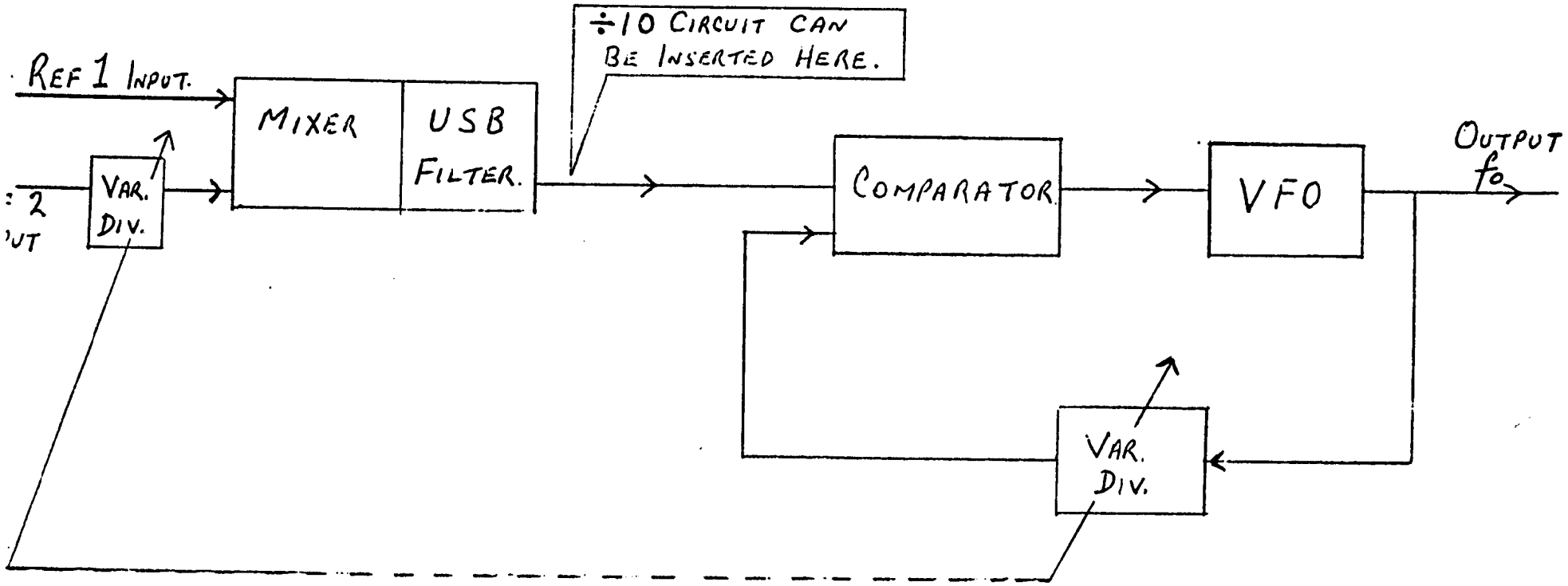


Fig (b) Development of Fig (a) Circuit.

A = (W x REF 1) = 40 x 1 = 40 MHz
B = 0.1(X+A) = 0.1(50+40) = 9 MHz
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D = (Z+C) = (70+6.9) = 76.9 MHz

10.2.5 Table 1 shows the effect of varying terms W, X,Y and Z separately. By this method, four division ratio controls (one for each stage) can be calibrated in terms of digits of the output frequency fo. These controls can be further combined by external circuits into one single rotary knob.

TABLE 1 : VARIATIONS OF DIVIDER TERMS

Divider Term				Varied by	Varied by	Varied by	Varied by
W	X	Y	Z	Term Z	Term Y	Term X	Term W
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40	50	60	80	8 6	. 9	0	0 MHz
40	50	60	71	7 7	. 9	0	0 MHz
40	50	60	70	7 7	. 0	0	0 MHz
40	51	60	70	7 6	. 9	1	0 MHz
40.5	50	60	70	7 6	. 9	0	5 MHz

10.2.6 The range of variation of term Z is decided by the desired frequency range. The variations of terms Y and X are both over a range of ten. In the example given, the variation of term W is over a range of one in steps of 0.1 or less: in a practical circuit, term W is a division ratio of hundreds and therefore would vary over a larger range. The smallest step by which output frequency can be varied, so producing a circuit (Figure (c)) in which fine variations of frequency can be made, without incurring the penalty of long 'lock' time.

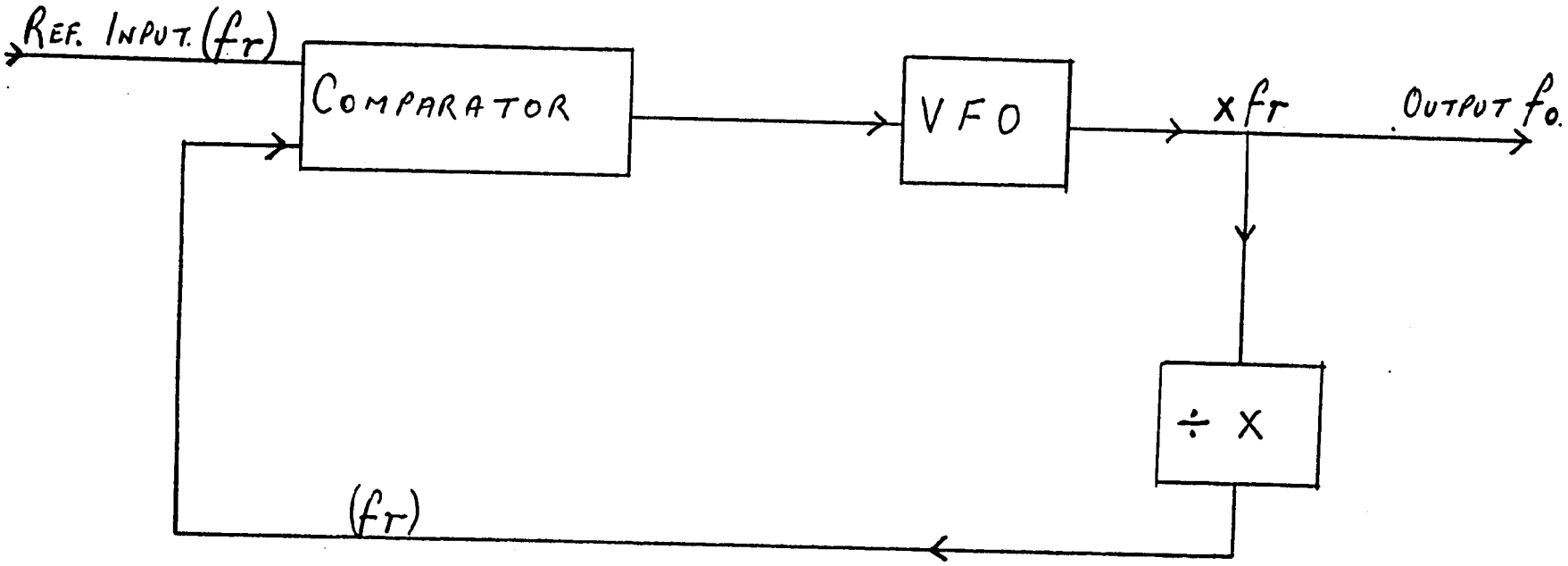


FIG. (a) BASIC PHASE-LOCK LOOP

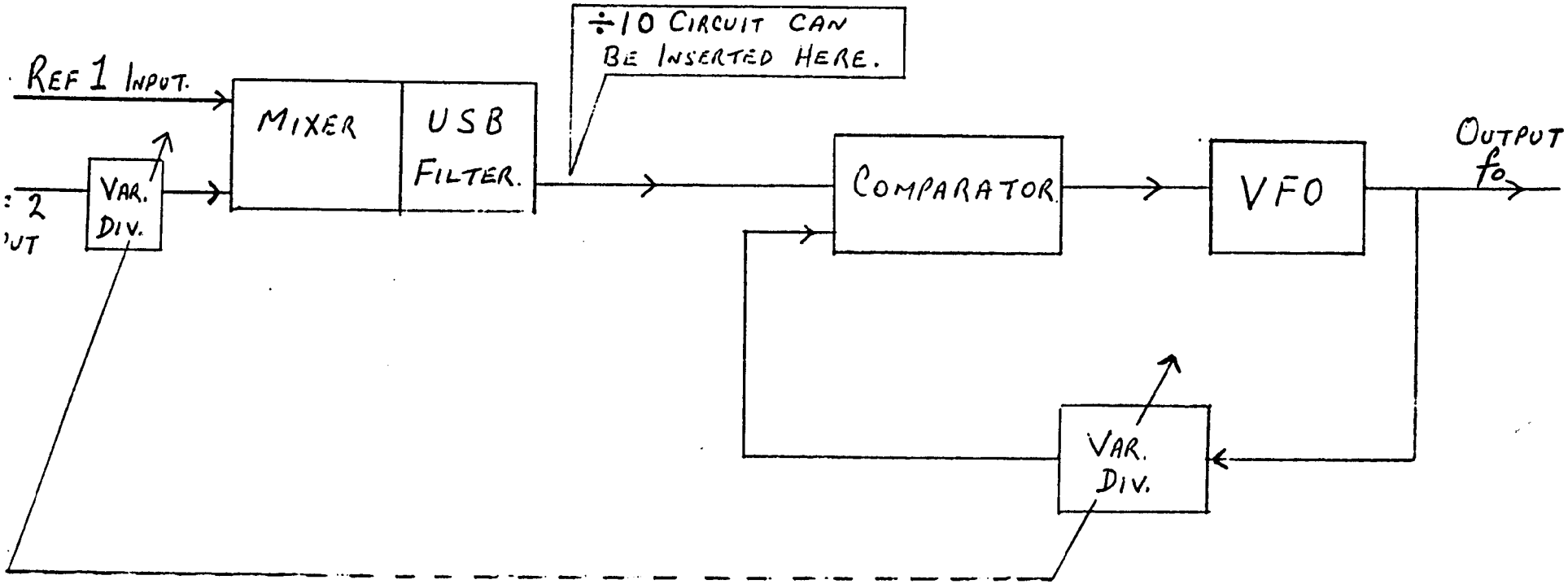


Fig (b) Development of Fig (a) Circuit.

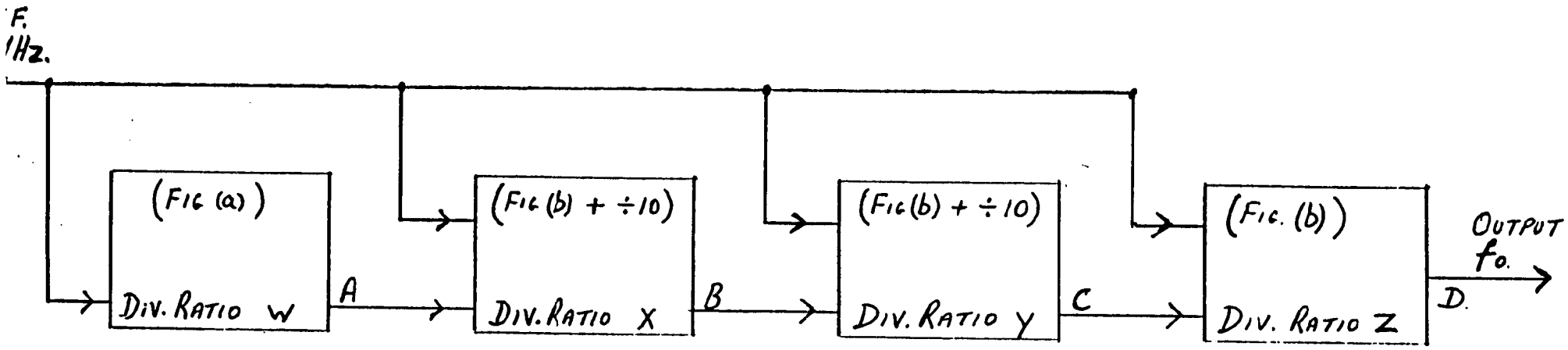
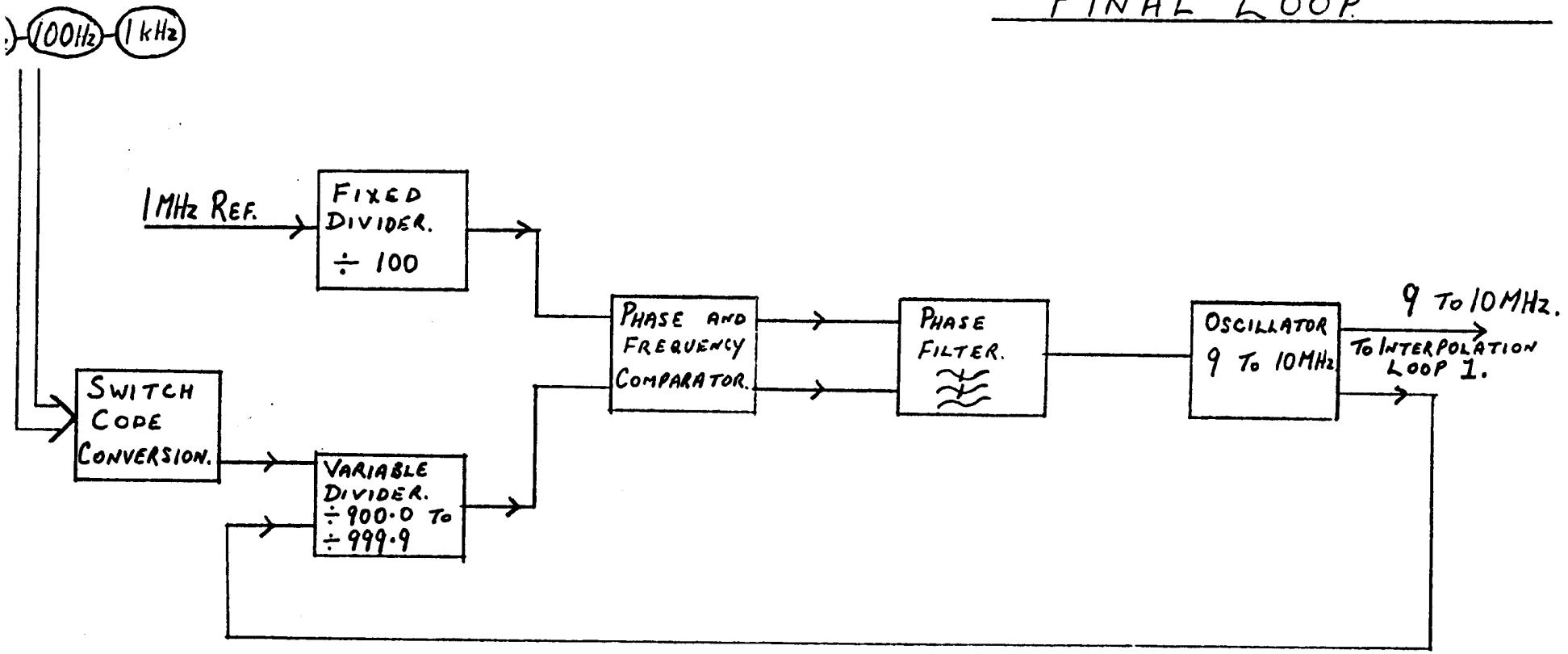


Fig. (c) Four - Term Cascade Phase-Lock Loop.

FINAL LOOP



MODULE 9A: SYNTHESISER.

10.3 Functional Description

10.3.1 1st Local Oscillator

10.3.1.1 The 1st local oscillator circuit is composed of four sections, with each section controlled by one of the divider terms W, X, Y, and Z. The term values are:-

W : 900 to 999.9 (FINAL LOOP)

X : 81 to 90 (INTERPOLATION LOOP 1)

Y : 81 to 90 (INTERPOLATION LOOP 2)

Z : 56 to 85 (OUTPUT LOOP)

Variations of term values for given final output frequency shifts are as shown in Table 2.

TABLE 2 : VARIATIONS OF TERM VALUES

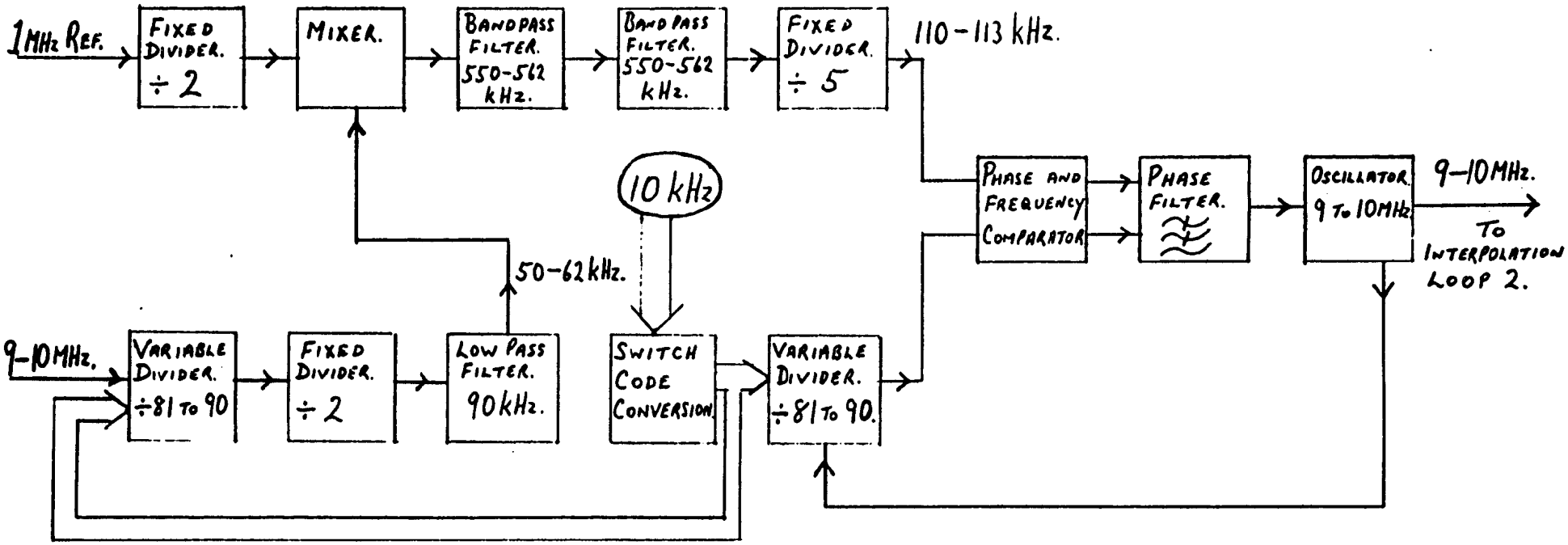
	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	1 MHz	10 MHz
W :	0.1	1	10	-	-	-	-
X :	-	-	-	1	-	-	-
Y :	-	-	-	-	1	-	-
Z :	-	-	-	-	-	1	10

The first stage consists of the 'FINAL LOOP' circuit and is of the form shown in Figure (a). The 1 MHz REF input is divided down to 10 kHz : this, in conjunction with a term W division ratio variable between 900 and 999.9 produces a FINAL LOOP output frequency between 9 and 10 MHz which can be varied in steps of 10 Hz, 100 Hz or 1 kHz.

10.3.1.2 The output from the final loop is applied to the second stage, known as INTERPOLATION LOOP 1: The circuit is of the form shown in Figure (b) with the addition of a divide-by-ten circuit as previously described. Term X value is variable between 81 and 90: this, in conjunction with a 9 to 10 MHz input from the FINAL LOOP produces an output frequency between 9 and 10 MHz. A variation of one in term X produces an interpolation loop 1 output frequency variation of 10 kHz. The Interpolation loop 1 output frequency, therefore, is between 9 and 10 MHz and can be varied in steps of 10 kHz, 1 kHz, 100 Hz and 10 Hz (equivalent to output B in Figure (c)).

10.3.1.3 The output from the interpolation loop 1 is applied to the third stage, known as interpolation loop 2; this is identical with interpolation loop 1 and is housed on three similar printed circuit panels. A variation of one in term Y produces an interpolation loop 2 output frequency variation of 100 kHz. The output frequency is between 9 and 10 MHz and can be varied in steps of 100 kHz, 10 kHz, 1 kHz, 100 Hz and 10 Hz (equivalent to output C in Figure (c)).

Interpolation Loop 1.



Module 9A: Synthesiser.

10.3.1.4 The output from interpolation loop 2 is applied to the fourth stage known as the OUTPUT LOOP: the circuit is of the form shown in Figure (b), and no divide-by-ten action occurs. Although a divide-by-ten function exists on the reference input to the comparator, this is nullified by a divide-by-ten circuit placed on the variable divider line. The action therefore becomes the mathematical addition of term Z (MHz) to the output from interpolation loop 2 (MHz). A variation of one in term Z produces a 1 MHz output frequency step. The OUTPUT LOOP output frequency, therefore is between 65 and 95 MHz and can be varied in steps of 10 MHz, 1 MHz, 100 kHz, 10 kHz, 1 kHz, 100 Hz and 10 Hz.

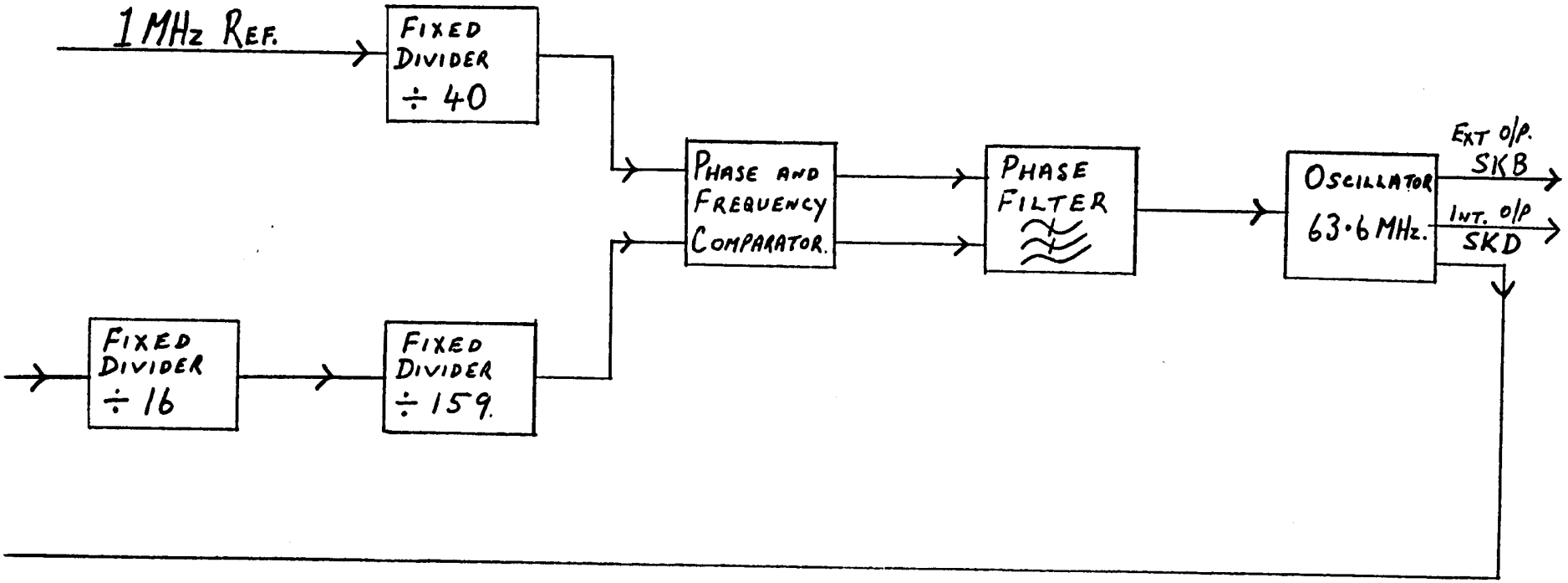
10.4 2nd Local Oscillator

10.4.1 The fixed-frequency 2nd local oscillator is housed on panels K and L. It consists of a circuit of the form shown in Figure (a) with a divider in the reference input line. An output frequency of 63.6 MHz is produced.

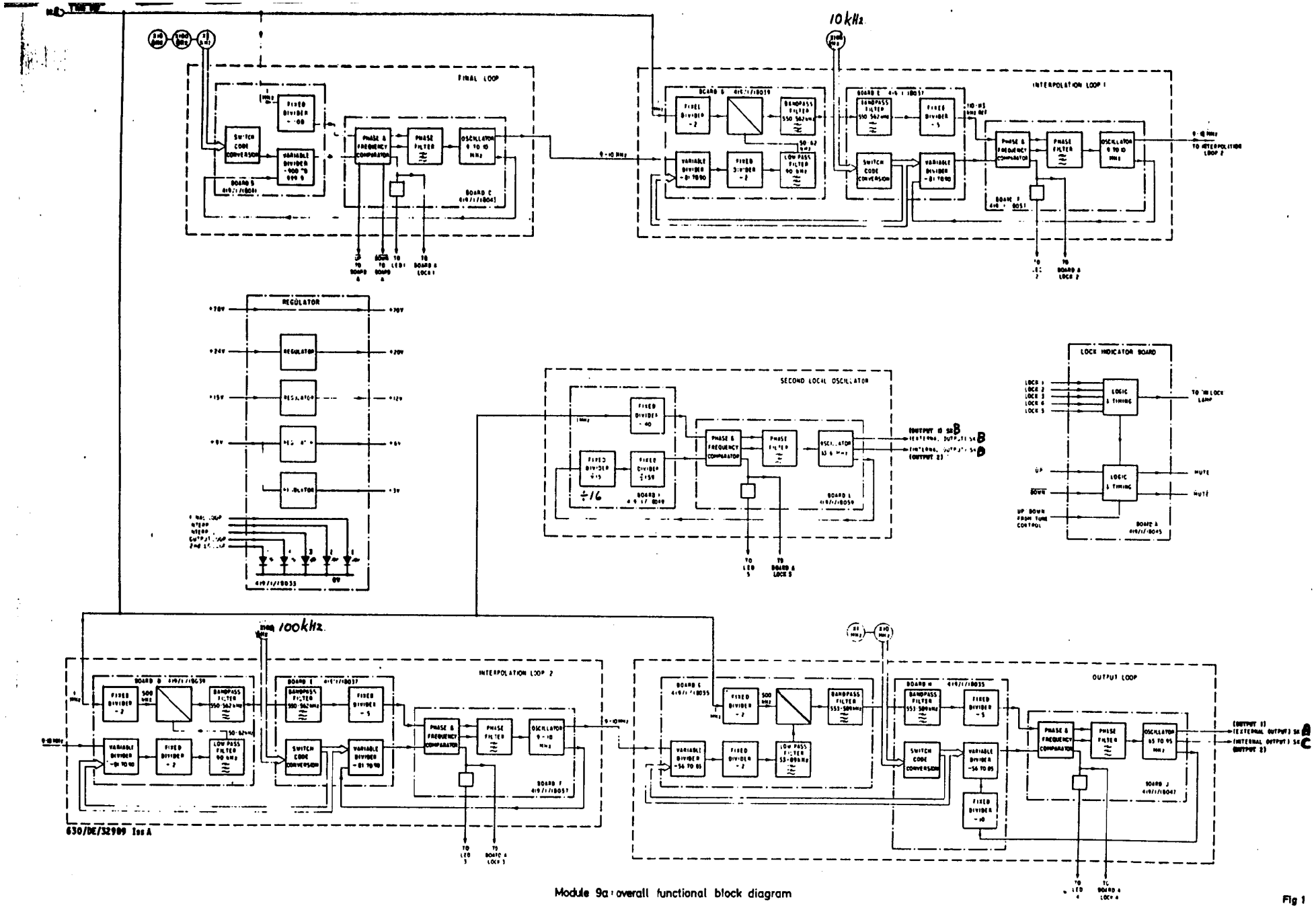
10.5 Monitoring

10.5.1 A monitor output is taken from the Phase and Frequency Comparator of each phase-lock loop. A LED indicator is provided for each of the five loops, indicating when it is in lock. When all are in lock, a further LED indicator indicates 'all in lock'. When tuning (ie frequency variation) is in progress lock is lost; under these conditions a muting output is produced which shuts down the receiver outputs until lock is acquired on the new tuning setting. The monitoring circuits are housed in panel A.

SECOND LOCAL OSCILLATOR.

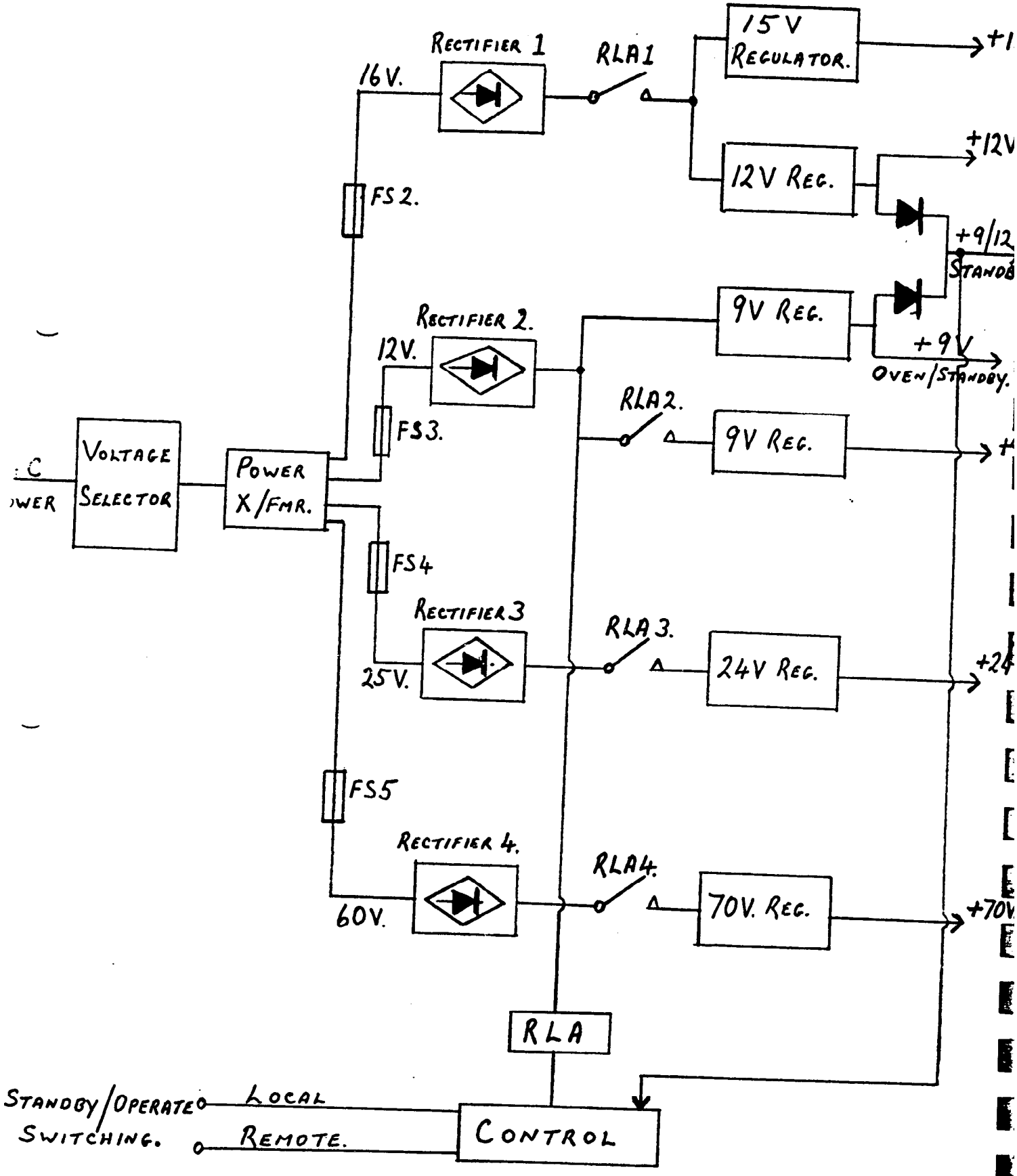


MODULE 9A: SYNTHESISER.



Module 9a : overall functional block diagram

Fig 1



MODULE 8C: POWER SUPPLIES

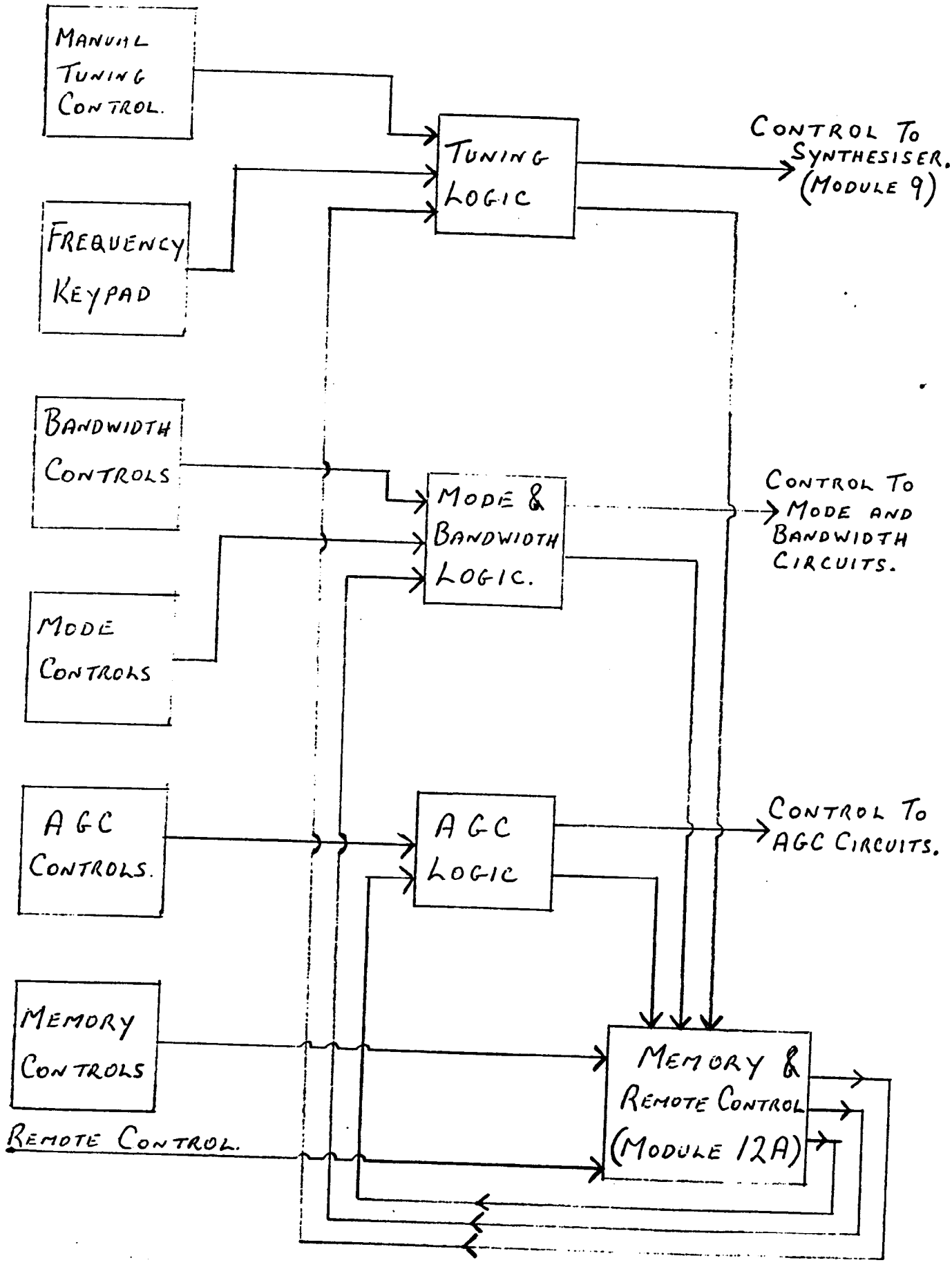
11. MODULE 8C : POWER SUPPLIES

11.1 Functional Description

11.1.1 Module 8C is the Power Supply Unit, operating from a 45 to 400 Hz single-phase AC supply of either 100 to 125V, or 200 to 250V. Power consumption is approximately 90VA.
DC power outputs are +9V, +12V, +15V, +24V and +70V.

11.1.2 Four bridge rectifiers are fed from the power transformer, each rectifier having a reservoir capacitor with discharge resistor and one or two voltage regulating circuits. In the receiver 'standby' stage, AC power is applied, Relay A is not energised, and only one of the 9V regulators gives an output (+9/12V STANDBY), this supplies the control logic circuitry. Relay RLA is powered by the raw 12V rectifier output and operated by the control logic.

11.1.3 On switching the receiver from STANDBY to OPERATE, RLA is energised and rectified DC is applied to the remaining five regulators, all DC outputs are then available. In addition, the +9V/+12V STANDBY output voltage rises from +9V to +12V.



MODULE 10J: BASIC FUNCTIONAL DIAGRAM.

12. MODULE 10J : FRONT PANEL AND CONTROL CIRCUITS

12.1 Introduction

Module 10 embraces the front panel of the PR 2250 receiver and the circuit-board mounted upon it. These two items together embody all the digital logic which forms the interface between the operator and the receiver proper. The logic operates in conjunction with the memory circuits in Module 12A.

12.2 Basic Functional Description

12.2.1 Frequency Control

The operator controls frequency either by using the keypad or by use of the optical encoded manual tuning control. Provision is also made for recalling frequencies stored in the memory. These three sources generate the control input to the tuning logic. The tuning logic output determines the frequency of the synthesiser (1st LO). In addition, a frequency data output is fed to the memory circuits.

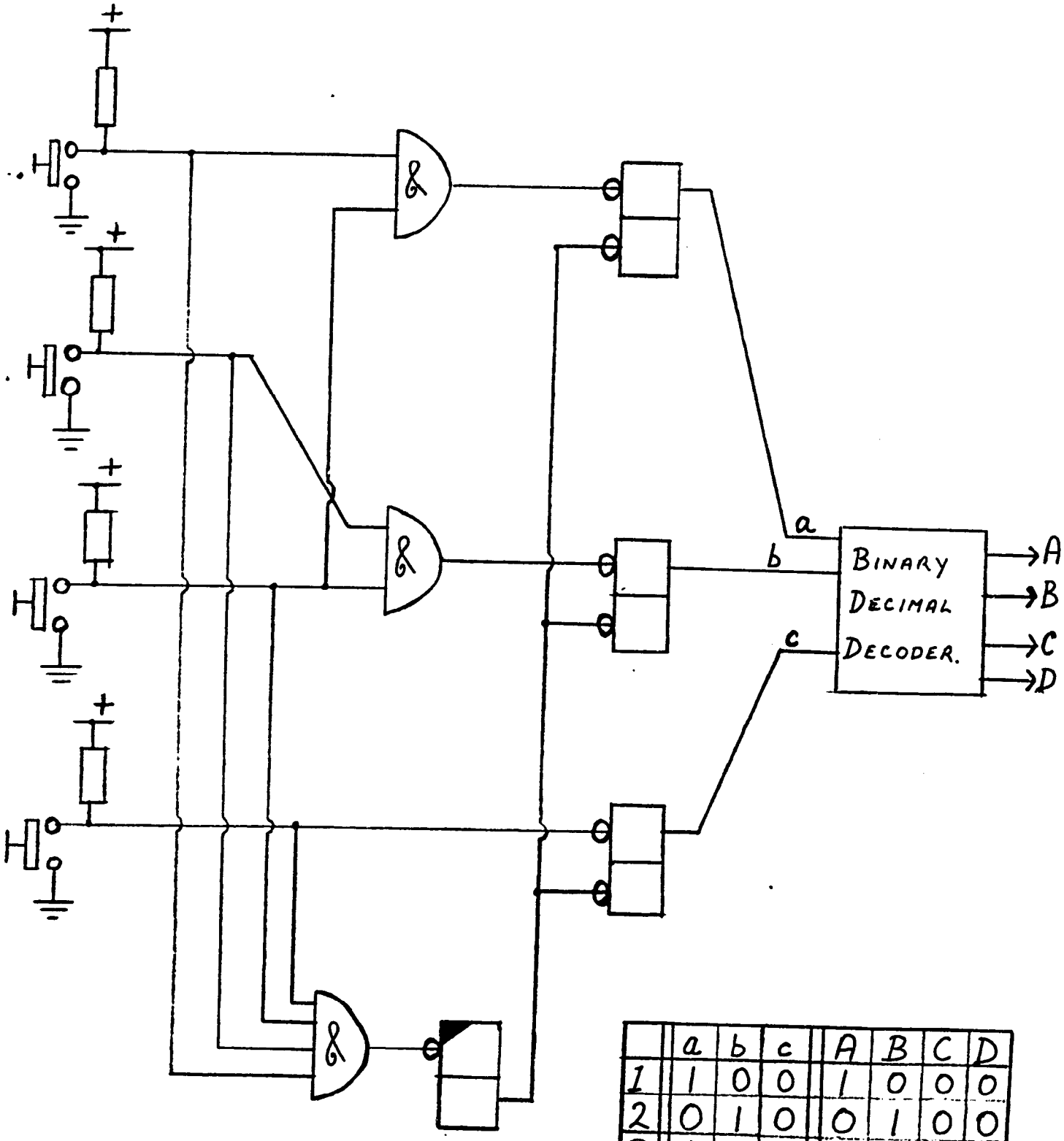
12.2.2 Mode and Bandwidth Control

The mode and bandwidth controls are to a certain extent interdependent, in as much as selecting some modes automatically selects the appropriate bandwidth. However, where this is undesirable, the automatically selected bandwidth setting can be manually over-ridden. The mode and bandwidth logic also generates an input for the memory.

12.2.3 AGC Control

AGC decay time-constant is operator selected. The selected value is fed to the AGC circuits and the memory.

MODULE 10J : KEYPAD.



	a	b	c	A	B	C	D
1	1	0	0	1	0	0	0
2	0	1	0	0	1	0	0
3	1	1	0	0	0	1	0
4	0	0	1	0	0	0	1

FIG (b) BASIC PUSH-BUTTON SYSTEM.

12.2.4 Memory Control

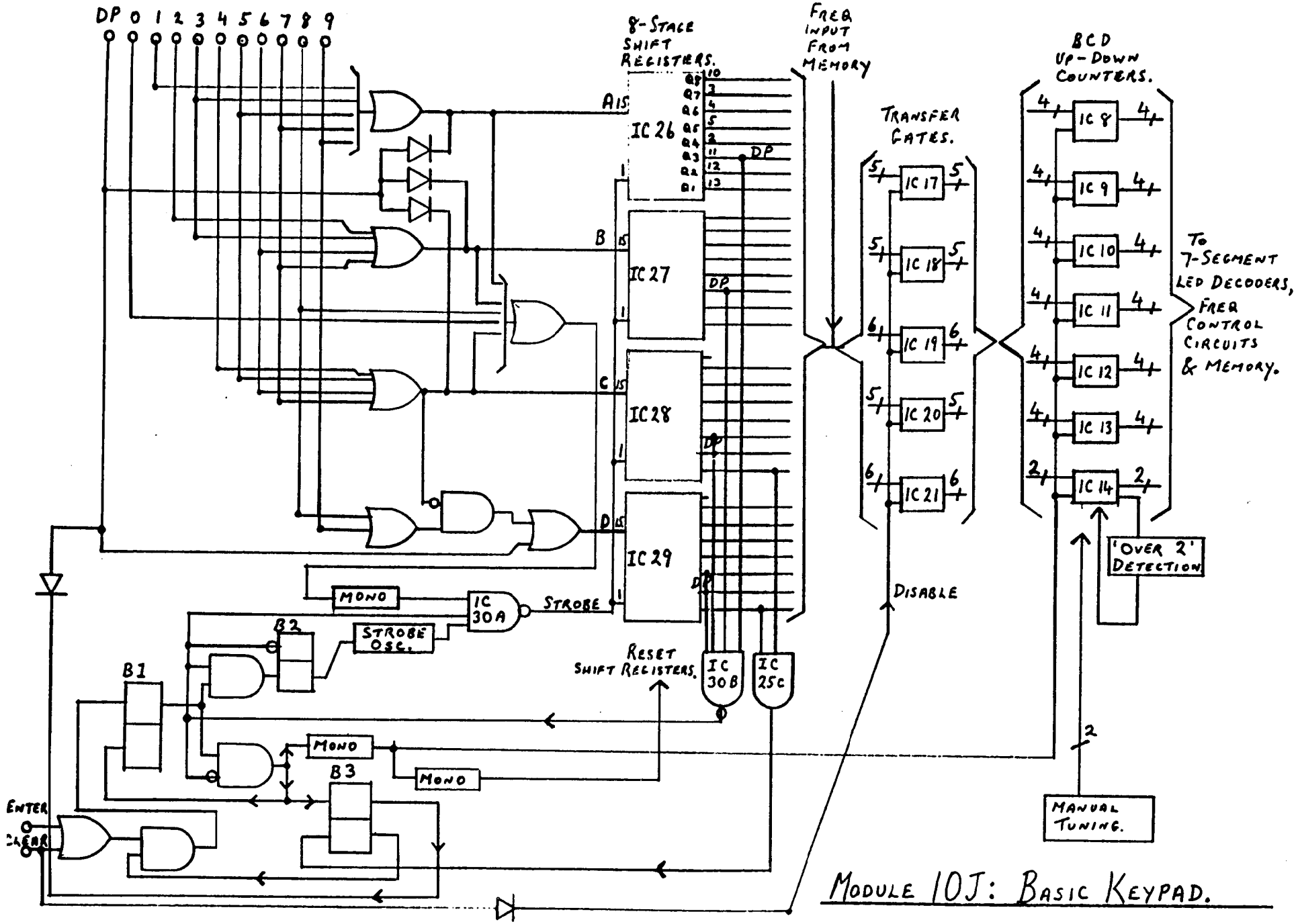
The memory has 16 storage channels. The memory is battery maintained, and will hold data for several months while the receiver is switched off. Recall facilities allow any stored set of data to be instantly applied to the receiver controls.

12.3 Push Button Control

12.3.1 Apart from the manual tuning and some switches, all other operator controls are 'press to operate' buttons. The basic system can be seen in Figure (b). Operation of any button triggers the monostable, producing a very short '1-0-1' output pulse and also applying a '0' set level to one or more bistables. Those bistables which do not receive a '0' set level are reset by the short duration monostable output pulse, which ends before the operator releases the button. In the period between the end of the monostable output pulse and the button release, one or more bistables are set.

12.3.2 In Figure (b) a four-button circuit is shown. Button 1 produces binary 1 at a, b, c; Button 2 produces binary 2 and so on. The binary number set into the bistables is decoded to produce a '1' level on one output of the decoder. The system is applicable to any number of buttons by use of suitable "AND" gating and sufficient bistables to store the largest binary number required.

12.3.3 As an example, Push-Button 4 in Figure (b); the monostable produces a short '1-0-1' pulse which resets the upper two bistables. It cannot reset the lower bistable because of the '0' set level applied by Button 4.


DP 0 1 2 3 4 5 6 7 8 9
8-STAGE SHIFT REGISTERS.
FREQ INPUT FROM MEMORY
BCD UP-DOWN COUNTERS.
TRANSFER GATES.
IC 26
IC 27
IC 28
IC 29
IC 17
IC 18
IC 19
IC 20
IC 21
IC 8
IC 9
IC 10
IC 11
IC 12
IC 13
IC 14
TO 7-SEGMENT LED DECODERS, FREQ CONTROL CIRCUITS & MEMORY.
'OVER 2' DETECTION
DISABLE
MONO
IC 30A
STROBE
STROBE OSC.
B1
B2
B3
RESET SHIFT REGISTERS.
IC 30B
IC 25C
ENTER
CLEAR
MANUAL TUNING.
MODULE 10J: BASIC KEYPAD.

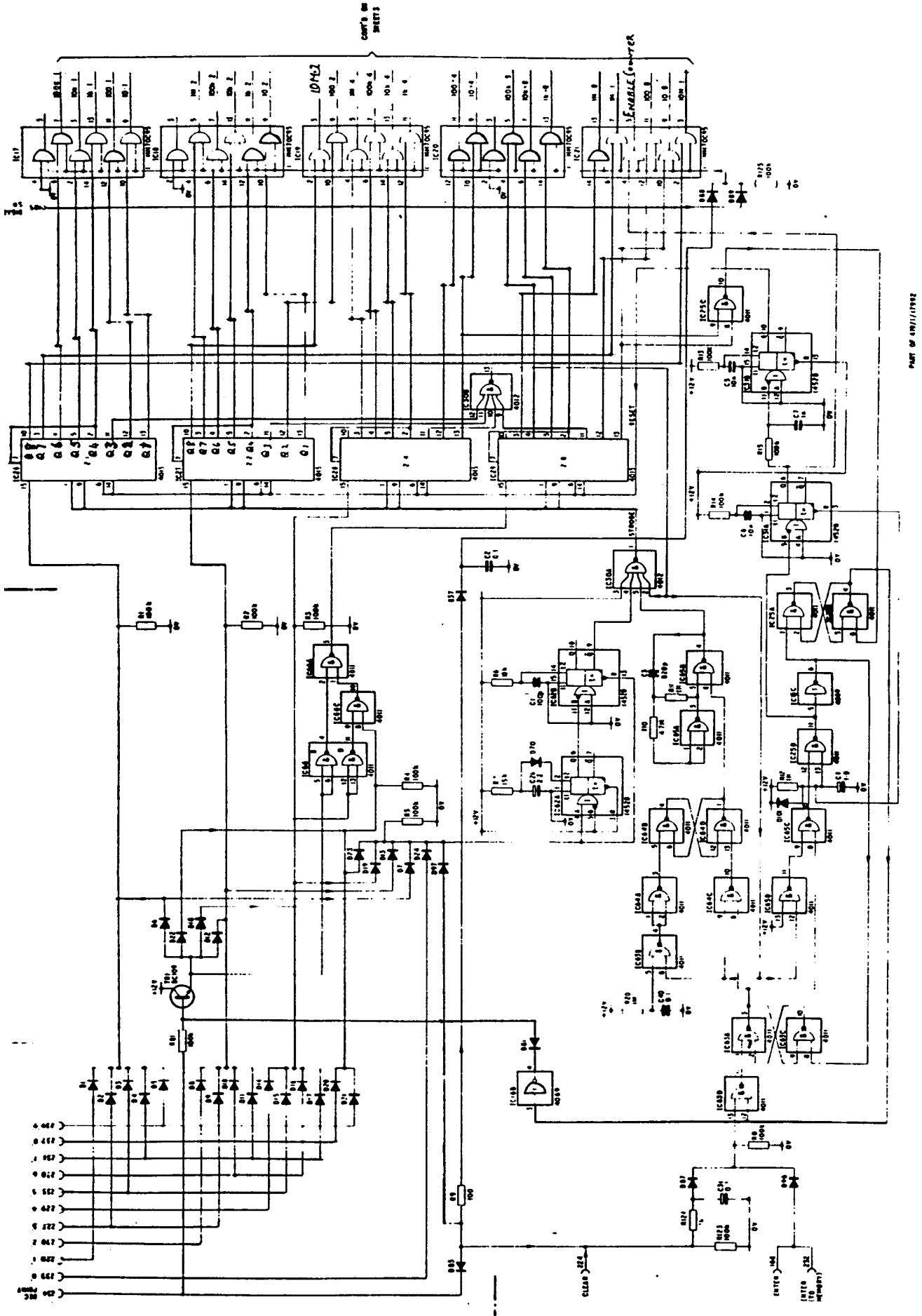
After the end of the monostable output pulse, the button will still be held. During this period, the lower bistable is set, producing a - 0, b - 0, c - 1 ie binary 4 in parallel form. This binary 4 will remain stored in the bistables until another button is pressed: it is decoded to produce a '1' output on line D.

12.4 Keypad

12.4.1 On entering a frequency on the keypad numerical inputs, a logic '1' is fed through one or more 'OR' gates consisting of three bands of diodes to four 8-stage shift registers. The shift registers are IC26, IC27, IC28 and IC29. The inputs and outputs of the shift registers are in binary form. The first binary output will appear at Q1 of the shift registers. On receipt of the next entry from the keypad the first output on Q1 moves to Q2 and the second entry takes up position on the Q1 output of the shift registers. With each succeeding entry the output of the shift registers moves up one place.

12.4.2 To make a valid entry on the keypad the decimal point must be activated. Depressing the DP button activates a transistor and this produces a logic '1' at the Q1 outputs of all four shift registers. A logic '1' appearing at the Q1 outputs of IC28 and IC29 is sensed by IC25C, and via various ICs and the write diode D81, the transistor is switched off and held off, thus preventing further operation of the decimal point key. Whether further numerical entries were or were not made after the decimal point entry does not affect the operation so, for simplicity, we will assume there were none.

12.4.3 The next operation is to press the ENTER button. This in conjunction with a level '1' (due to the decimal point) causes a STROBE PULSE from IC30A to CLOCK the



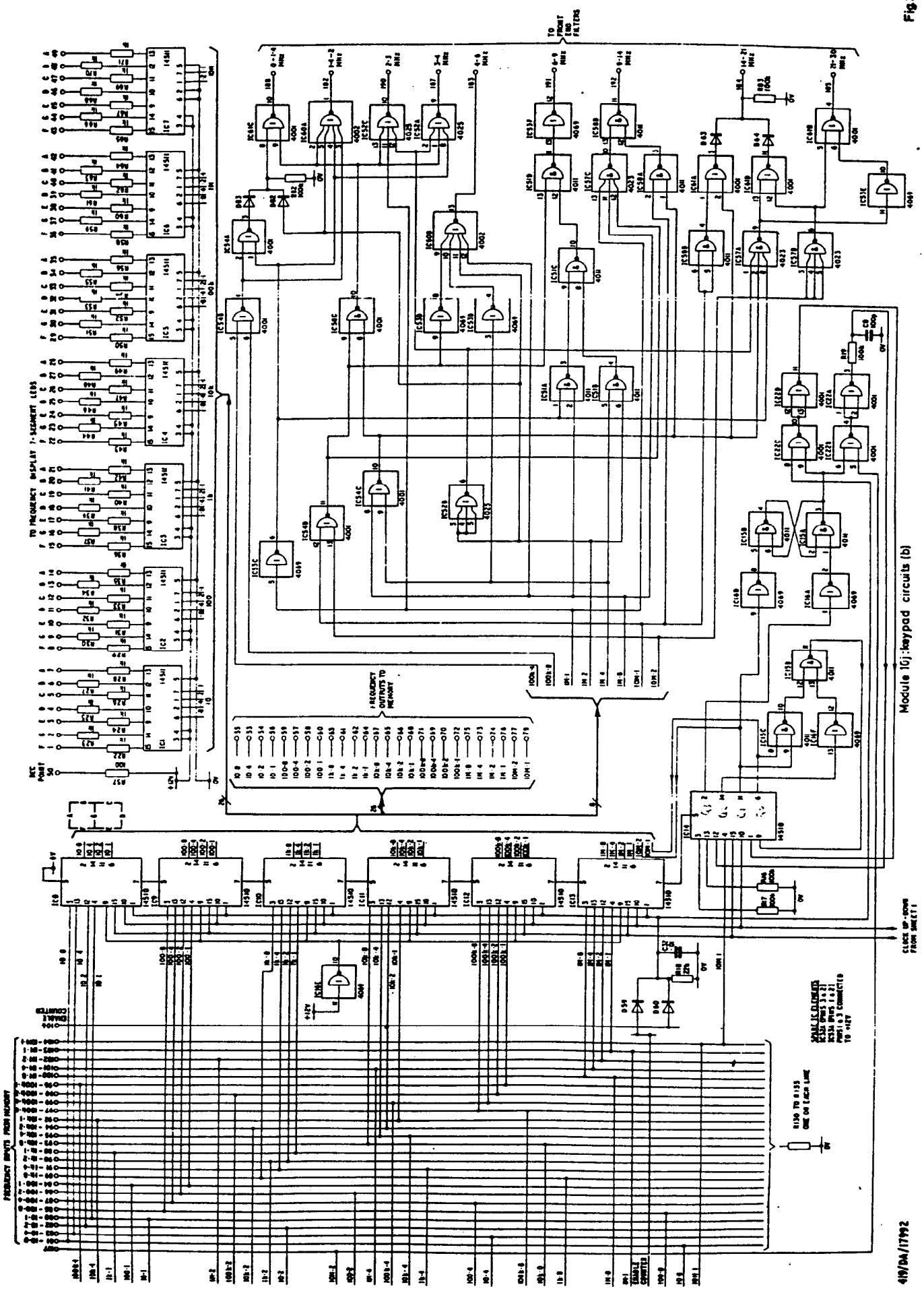

TO FRONT END FILTERS
TO FREQUENCY DISPLAY 7-SEGMENT LEDS
FREQUENCY OUTPUTS TO MEMORY
FREQUENCY INPUTS FROM MEMORY
CLOCK UP-DOWN FROM SHEET 1
Module 10j: keypad circuits (b)
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Fig 2

Shift registers. When the decimal point (1-1-1-1) reaches the Q3 outputs from the shift registers it triggers IC30B. IC30B output level drops from '1' to '0' and the strobe oscillator stops. The entries mode on the keypad are now in the correct position in the shift registers to operate the display decoders and produce a meaningful output to the synthesiser. This is done via BCD UP/DOWN counters which, for keypad entries, merely act as stores.

12.4.4 At the same time as the strobe oscillator stops, the combination of IC30B output at '0' and IC63A output at '1' has three effects:

(1) The two monostables, IC31A and IC31B are fired. The first one applies a preset to the up-down counters (IC8 to 14) allowing the register outputs to appear on the counter outputs. The transfer gates IC17 to IC21 are normally transparent to data. There is delay on the second monostable which, a little later, resets the shift registers ready for the next entry.

(2) IC63A output is set to '0' which is the start state for another operation.

(3) IC25B output is set to '0' which removes the 'hold' from the transistor in the decimal point line which is the start state for another operation.

12.4.5 The connection between the shift registers and the up-down counters is made via transfer gates which are normally transparent to data. Their function is to break the connection when clearing an erroneous keypad entry. If, after a keypad numerical entry has been made but before the ENTER button is operated, it is desired to 'start again', the CLEAR button is

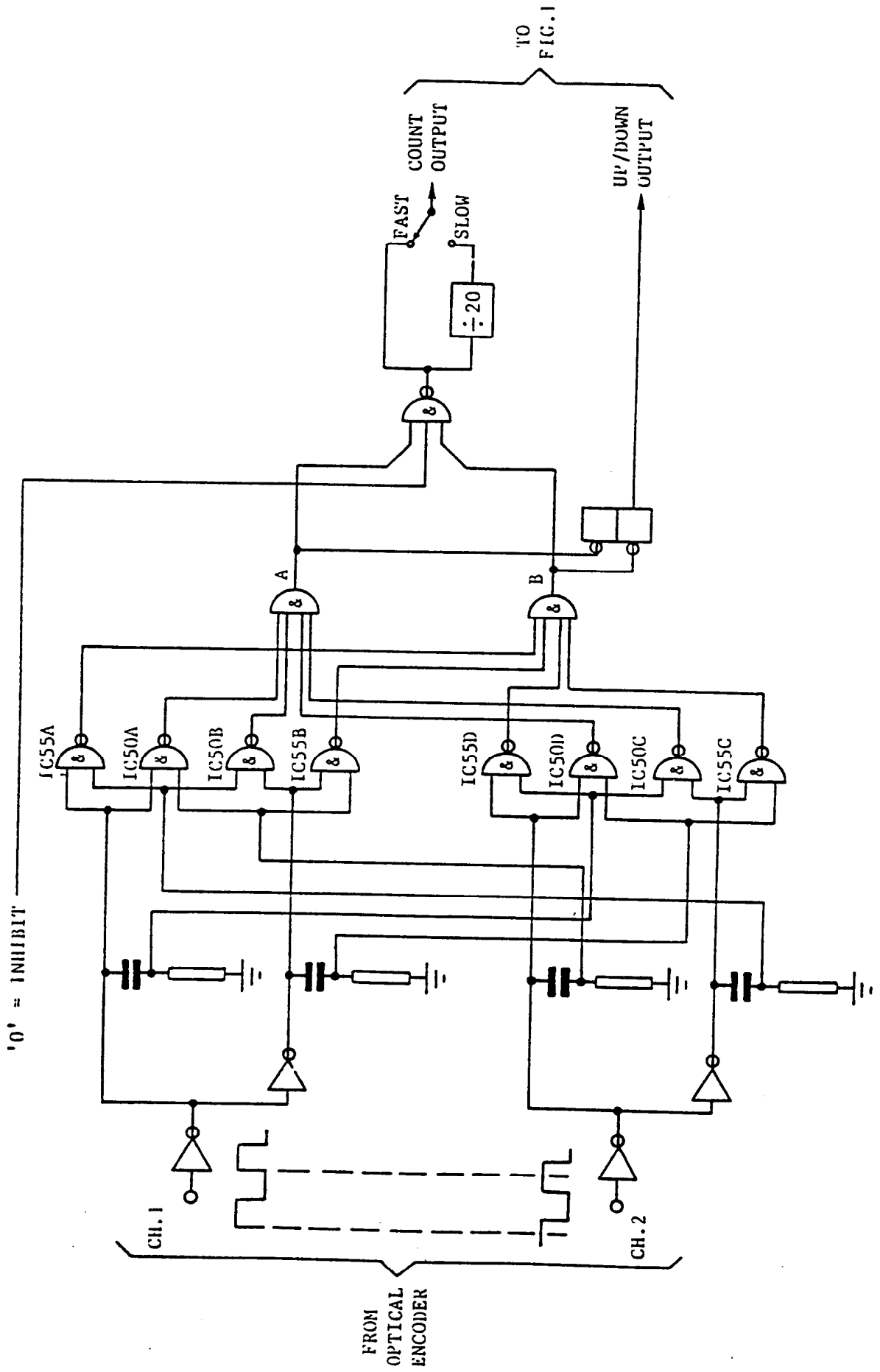


FIG (e) BASIC MANUAL TUNING LOGIC

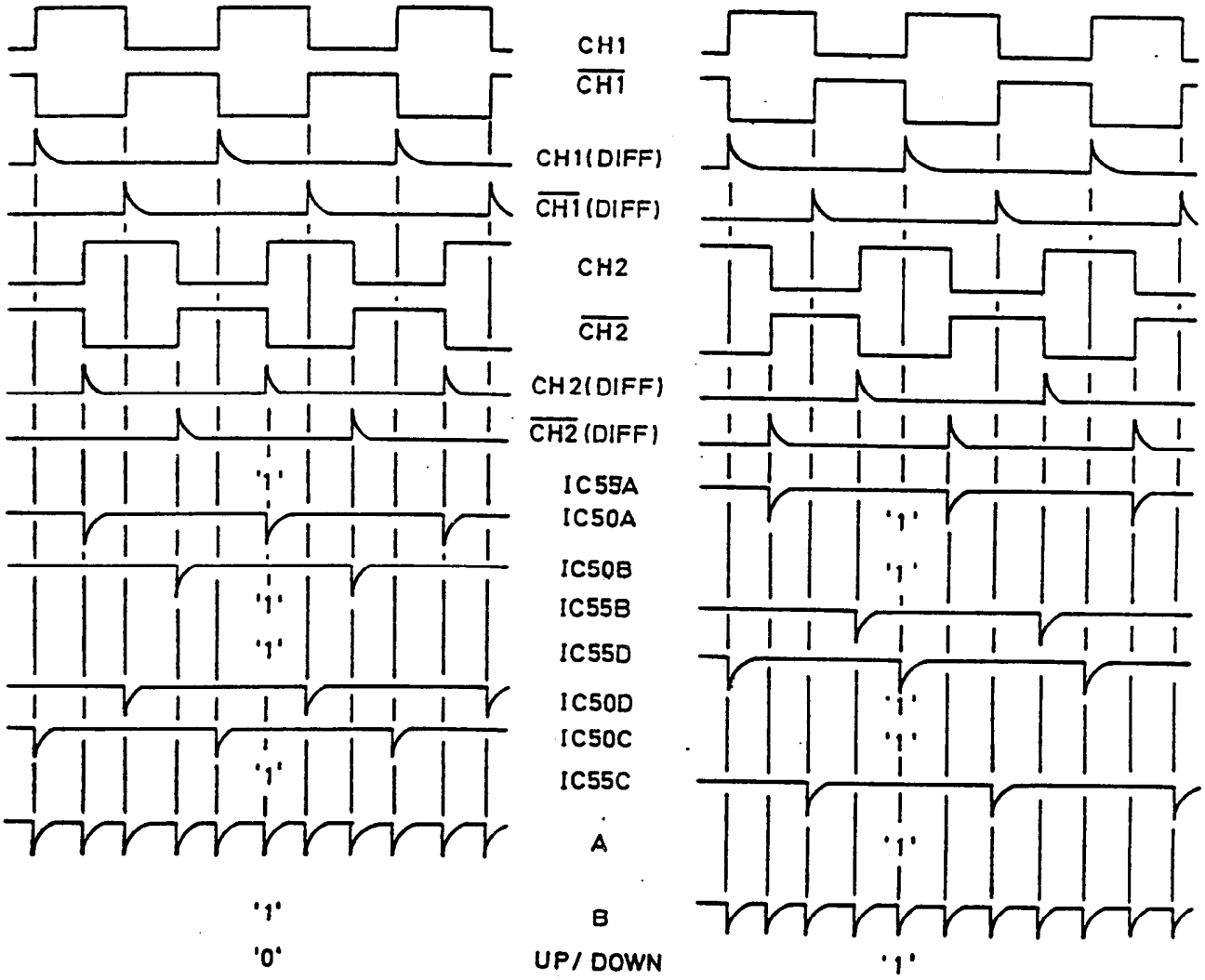


FIG (f) MANUAL TUNING CIRCUIT ACTION

pressed. This functions exactly as the enter button but with one additional action, which is to disable the transfer gates and prevent the incorrect entry from appearing at the counter outputs.

12.4.6 The up-down counters consist of IC8 to IC14. IC14 of the counter deals with the '10 MHz' digit. This must not exceed 2, as the maximum frequency is 29.99999 MHz. An 'over 2' detector comprised of IC15C and IC15D senses the output from IC14: if it exceeds binary 2 due to incorrect keypad entry, then the detector resets IC14 to bring its output within the range of the receiver.

12.4.7 The outputs of the up-down counters are in parallel BCD, and define the frequency in kHz. The output controls four functions.

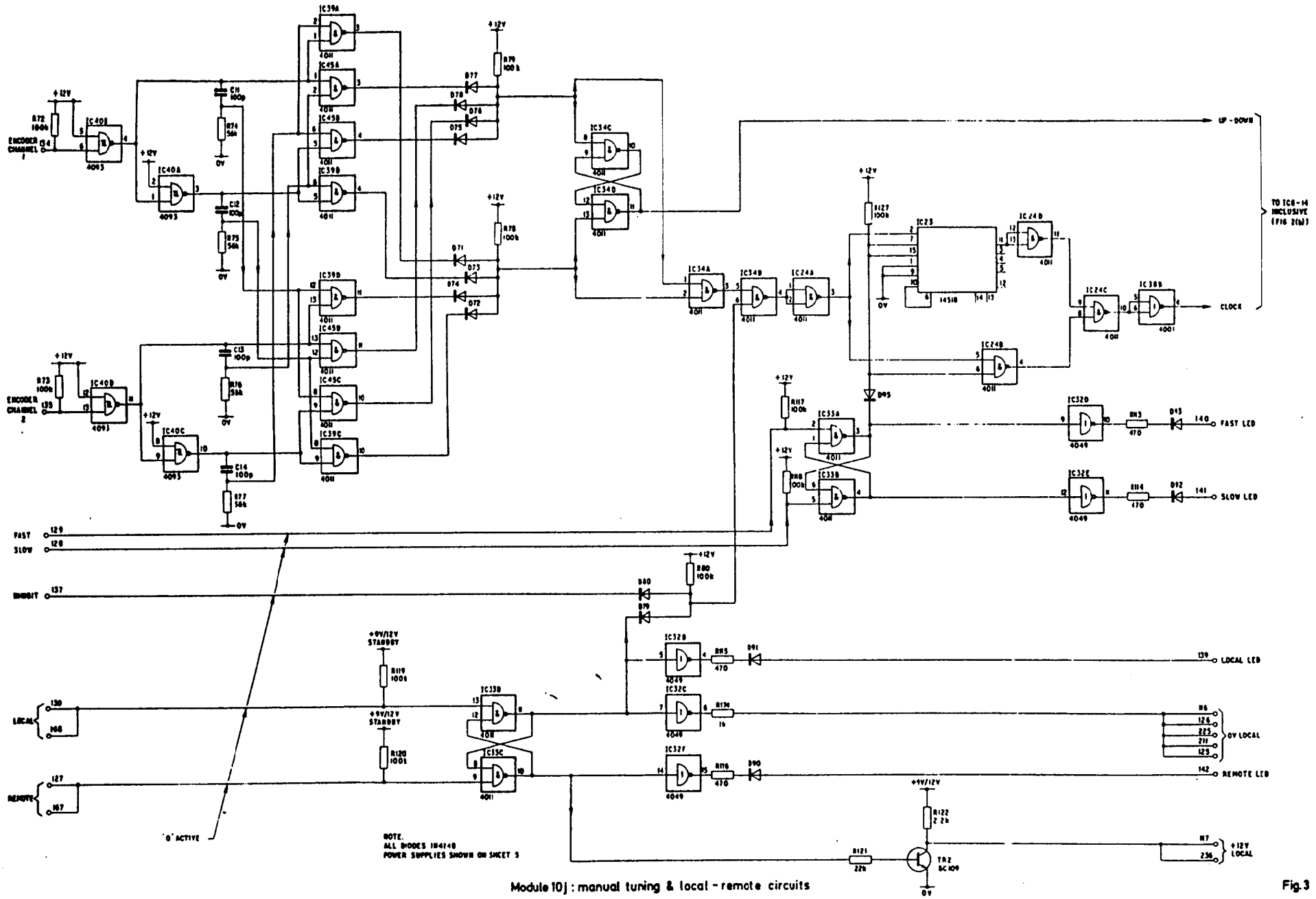
(1) THE SYNTHESISER FREQUENCY CONTROL UNIT (MODULE 9A)

(2) LED DECODERS OF THE FRONT-PANEL FREQUENCY DISPLAY (MODULE 10J)

(3) MEMORY CIRCUITS OF MODULE 12A

(4) FILTER-SWITCHING LOGIC CONTROLLING MODULE 1 (NOT USED)

12.4.8 The outputs from the up-down counters are fed out of Module 10J to the memory circuits and the frequency control circuits. Inside Module 10J they are applied to seven BCD 7-segment LED decoders (IC1 - IC7). These devices drive the front-panel frequency display. The decimal point on the display is a separate LED which is permanently illuminated via R57.



Module 10j : manual tuning & local - remote circuits

Fig.3

12.5 Manual Tuning

12.5.1 The optical encoder is driven by the manual tuning knob and uses a 12V d.c. supply to produce two square-wave outputs, 'Channel 1' and 'Channel 2': these outputs have a 90° phase relationship and at worst case, have a '1' level value of +12V and a '0' level value of 0.3V nominal. On each channel, 500 pulses are produced per encoder revolution.

12.5.2 The two outputs from the encoder are 'cleaned' by trigger inverters IC40B and IC40D. Two further trigger inverters IC40A and IC40C provide inverted signals. The output from each of the four trigger inverters is applied to a CR differentiation circuit. Each of the two encoder outputs is therefore available in four forms:

(a) Direct

(b) Inverted

(c) Direct differentiated

(d) Inverted differentiated

This produces a total of eight inputs to a gating circuit formed by IC39 and IC45 together with diodes D71-D78. Two outputs are always produced: one is a train of '1-0-1' short pulses at four times encoder output pulse rate, while the second is a steady '1' level (Points A and B in Figure (c)). Reversal of control rotation direction reverses the two states. The two outputs are applied to a set-reset bistable and to a NAND gate. The bistable output level indicates direction of rotation, while the pulse train indication of rotational speed and quantity appears at the output of the NAND gate.

12.5.3 The output from the bistable is fed to the up-down inputs of IC8 to IC14, while the output from the NAND gate is applied to the clock inputs of IC8 to IC14. According to direction of control rotation, the numbers stored in the counters can be increased or decreased, so controlling the counter output values.

12.6 Mode and Bandwidth Control

12.6.1 The Mode and Bandwidth control circuit is a straightforward extension of the basic circuit shown in Figure (b). Two groups of press-buttons are employed, one for mode (F, CW, LSB, USB, ISB, AM, P) and one for bandwidth (8, 1.2, 0.3, 0.1 kHz). Each group is gated into three bistables. The two groups of inputs can be produced either by the front-panel buttons or from the memory.

12.6.2 The operation of the F, CW or AM mode buttons automatically sets up a particular bandwidth. However, this does not prevent subsequent selection of a different bandwidth.

12.6.3 Operation of the P mode button automatically selects 0.3 LSB bandwidth. The bandwidth, AGC and reconditioned carrier LEDs are extinguished. The preset conditions cannot be over-ridden.

12.6.4 A basic block diagram of the circuit can be seen in Figure (d). The two groups of bistables each produce a 3-bit binary number output which is decoded by the controlled circuits.

12.6.5 The functional diagram shown in Figure (d) omits one input to the basic circuit; this input is an inhibit on bistables D, E and F, which comes into operation when USB, LSB, ISB or P mode is selected. An '0' level output is taken from the mode LED outputs and fed via diodes D56, D57, D58 and D102 (see Figure 4, Chapter 10 Service Manual) and is applied as a permanent inhibit to the three bandwidth selection bistables for as long as the mode remains selected.

Note that, if during USB, LSB, ISB or P mode operation a bandwidth button is pressed it will select

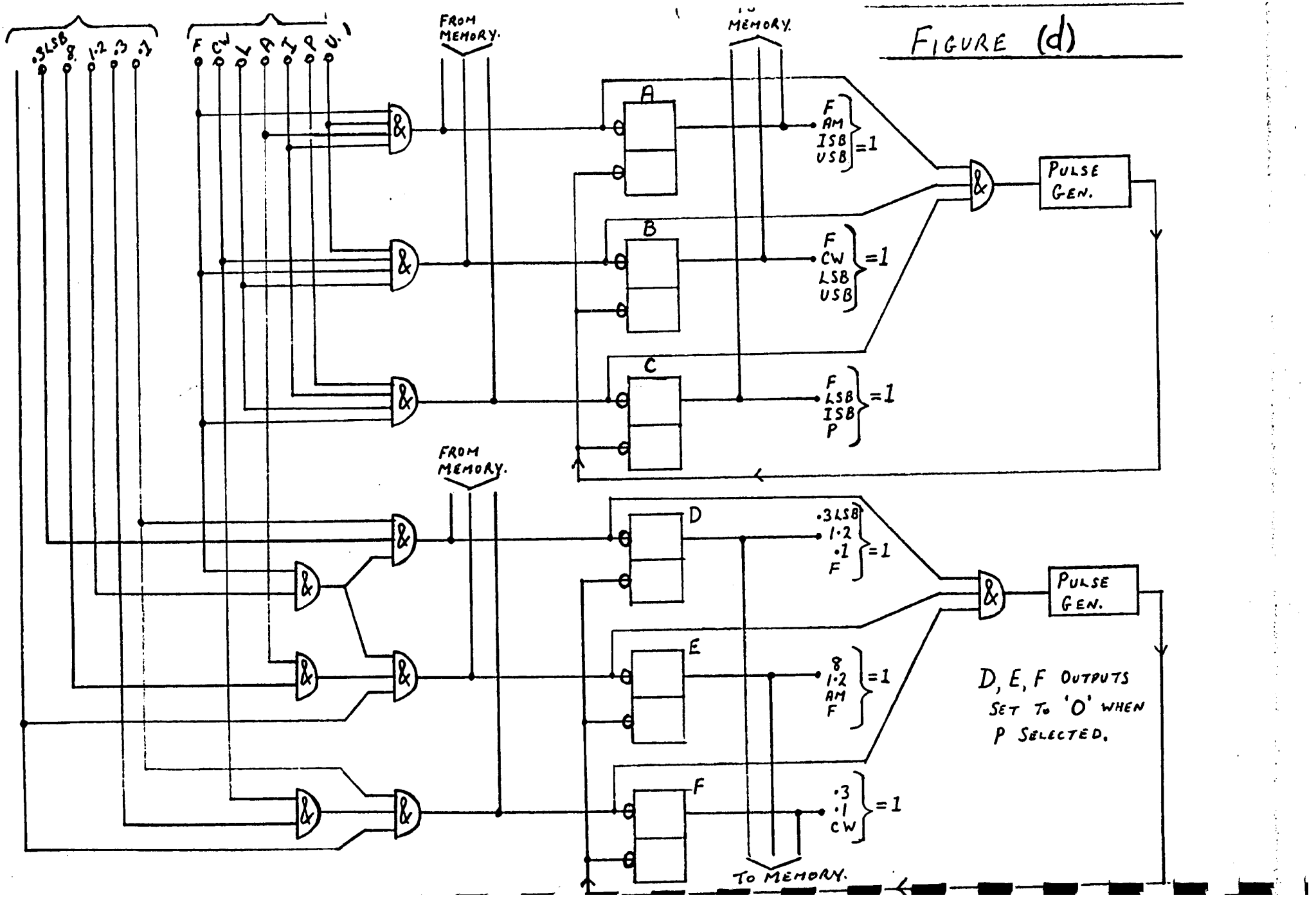
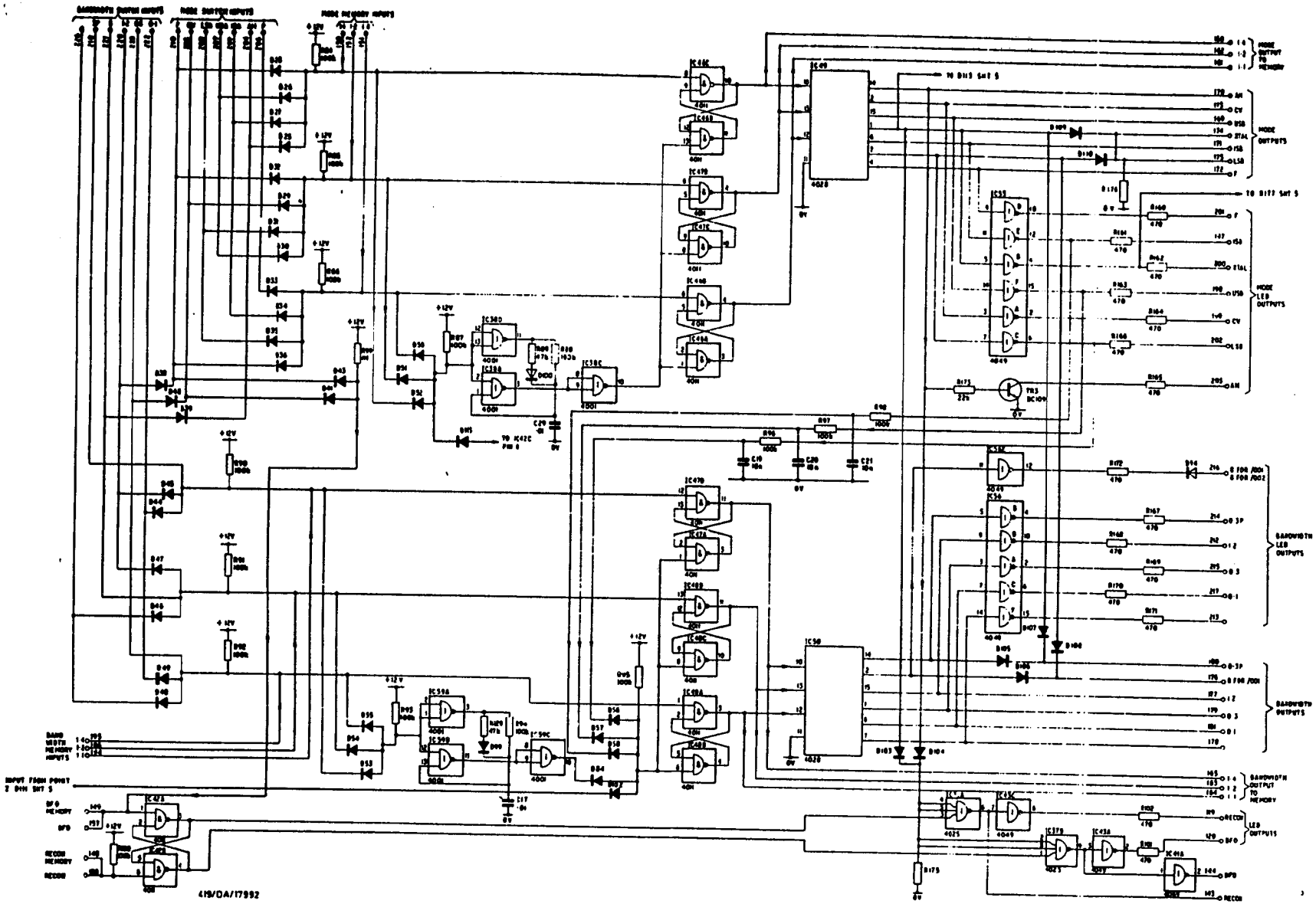


FIGURE (d)
.3LSB
.8
1·2
.3
.1
F
CW
LSB
AM
ISB
USB
P
FROM MEMORY.
TO MEMORY.
A
B
C
D
E
F
F AM ISB USB =1
F CW LSB USB =1
F LSB ISB P =1
.3LSB 1·2 .1 F =1
8 1·2 AM F =1
.3 .1 CW =1
PULSE GEN.
PULSE GEN.
D, E, F OUTPUTS SET TO '0' WHEN P SELECTED.
TO MEMORY.



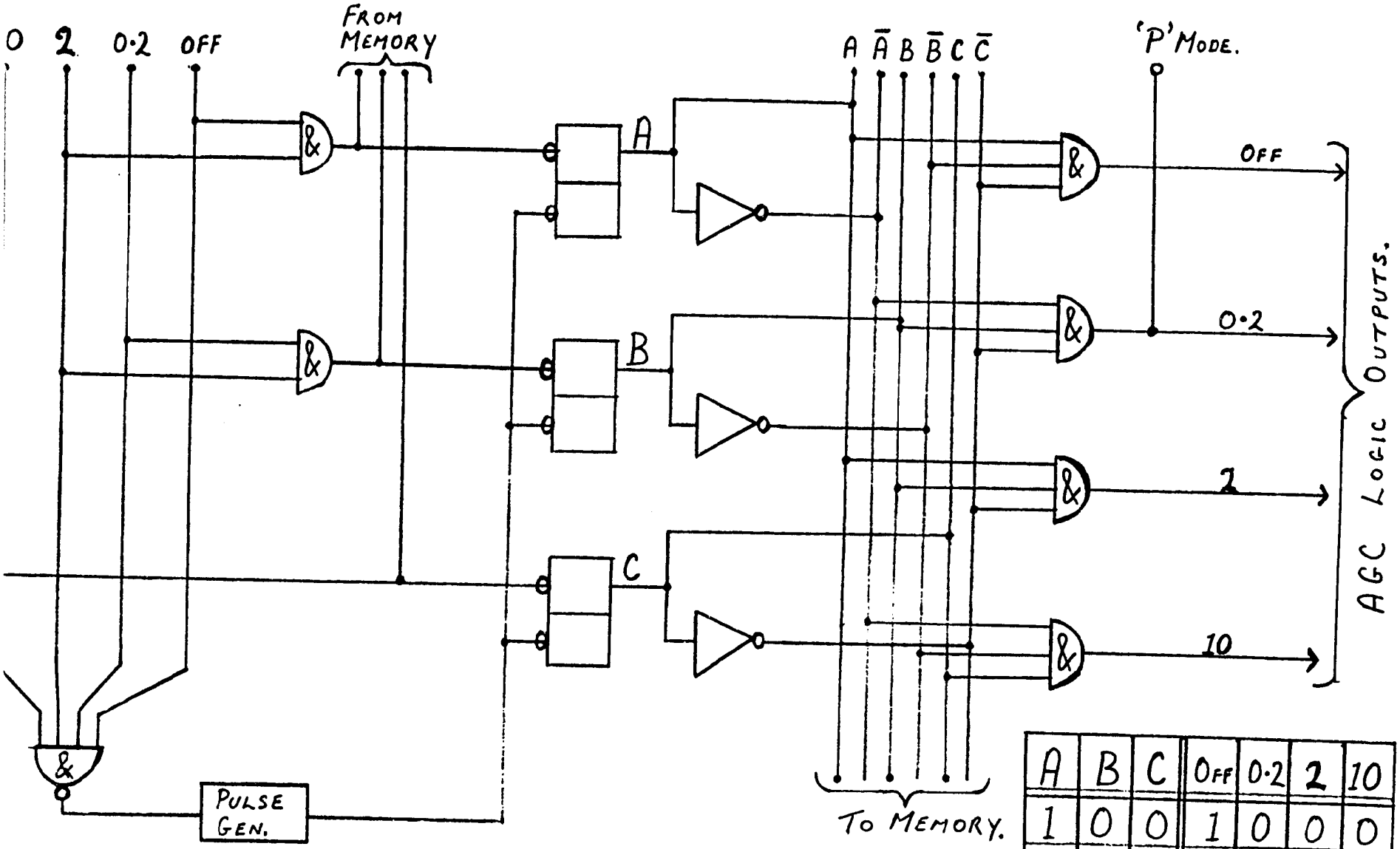
Module 10J : BFO, mode & bandwidth circuits

Fig 4

the appropriate circuit but will only do so while the button is pressed; this is not a valid mode of operation and is only mentioned to avoid this effect being mistaken for a fault condition.

12.6.6 Each of the two groups of bistables supply the inputs to a BCD - decimal decoder (IC49 and IC50). The output lines from each decoder are normally at '0'. One output line level rises to '1' according to the inputs applied.

12.6.7 The outputs from the decoders are the controlling inputs to the Mode and Bandwidth circuits, and are also fed via LED drivers IC55, TR3 and IC56 to operate the front-panel LED indicators. The mode and bandwidth outputs to the memory circuits are taken in parallel with the inputs to the decoders.



A	B	C	OFF	0·2	2	10
1	0	0	1	0	0	0
0	1	0	0	1	0	0
1	1	0	0	0	1	0
0	0	1	0	0	0	1

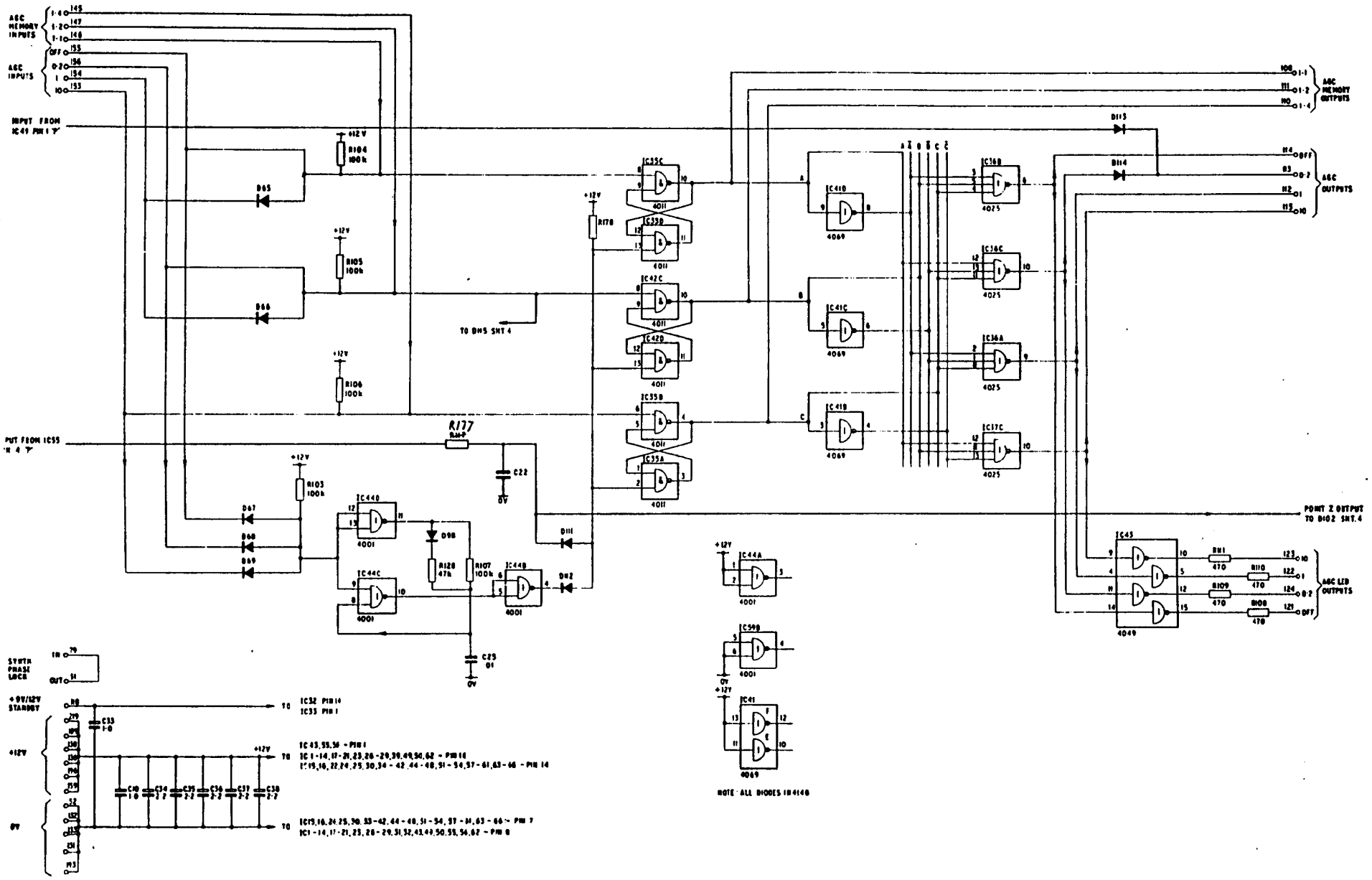
MODULE 10J: AGC CONTROL CIRCUIT.

12.7 AGC Control

12.7.1 As in the mode and bandwidth control circuits, the AGC selection circuit also uses push-button controlled bistables, Figure (e).

12.7.2 On operation of the AGC control button a level '0' is applied to the appropriate bistable A, B or C. The combined binary output is decoded by four AND gates, the outputs being fed to the control circuits, and to the front-panel LED indicators.

12.7.3 In mode 'P', SHORT AGC is automatically selected via IC49 and D113 (Service Manual, Chapter 10, Figure 4). The 'P' mode LED output - level '0' - is also applied via D111 to bistables A, B and C. This sets the bistable outputs to logic '0' and the AGC LEDs are extinguished.



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Module 10J: AGC & power circuits

Fig. 5

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